„Ge(Sn)-Based Vertical Gate-all-around Nanowire MOSFETs and Inverters for Low Power Logic“

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Abstract

Over the past half century, transistor miniaturization is the main driver to enhance Si complementary metal-oxide-semiconductor (CMOS) performance generation by generation in terms of shrinking the gate length, gate width, and oxide thickness, denoted as the Moore's Law. However, continuous advances of traditional planar devices hit a bottleneck because of power dissipation, packing density, electrostatic controllability and variability limitations. Approaches utilizing alternative channel materials and new device architecture, are proposed to further extend CMOS roadmap. Ge and newly emerging GeSn semiconductors are promising candidates because they offer high carrier mobilities, small and tunable bandgaps, and easy integration on Si wafers. Moreover, the migration of transistor architecture from conventional planar structure to 3D FinFET, and eventually to gate-all-around (GAA) nanowire device has been witnessed, which necessitates superior gate electrostatics and good immunity against short-channel effects. As is theoretically predicted, vertical GAA nanowire transistors provide further scalability, more layout efficiency and less power consumption compared to FinFETs and horizontal nanowire transistors, which are considered as the ultimate structure for the classical CMOS scaling.

This thesis investigates the application of vertical nanowires in the GeSn/Ge p-type and n-type MOSFETs and evaluates the feasibility of vertical nanowire transistors in logic circuit applications. In this regard, key process modules are examined: (i) An optimized vertical nanowire etching method for excellent verticality and smooth sidewalls is developed and digital etching, similar to atomic layer etching is applied to achieve nanowires with sub-20 nm diameters; (ii) Dielectric stacks with post-oxidation passivation are applied to reduce density of interface traps (D_{it}) between the dielectric and Ge(Sn) channel; (iii) Both p-type and n-type Ohmic contacts for Ge(Sn) are accessed for high performance MOSFETs.

Vertical Ge GAA nanowire pMOSFETs by a top-down approach are experimentally demonstrated for the first time, which exhibit excellent subthreshold properties. The superiority of gate electrostatic integrity is affirmed by the dependence of electrical performance on nanowire diameter scaling. The contact on the nanowire tip is revealed as the roadblock for vertical nanowire transistors. With the performance comparison by swapping source and drain, it is concluded that the doping deactivation effect in small nanowires is responsible for the performance asymmetry. Furthermore, low temperature I-V characterization manifests a typical temperature-dependence of subthreshold swing (*SS*), the deviation between experimental data and ideal *SS* lies primarily in D_{it} and source resistance.

Threshold voltage with temperatures depicts linear behaviors with slopes of 1.6 mV/K and 3 mV/K for 45 nm and 65 nm nanowire pMOSFETs, respectively.

To achieve enhanced on-state performance, $Ge_{0.92}Sn_{0.08}$/Ge GAA nanowire pMOSFETs are fabricated by growing GeSn as the top layer for a lowered contact resistivity. The strain distribution and band structure at the GeSn/Ge interface in the quasi-1D nanowires are calculated, which brings benefits for the key electrical figures of merits. With a scaled EOT of ~2 nm, GeSn/Ge nanowire pMOSFETs achieve low *SS* of 67 mV/dec, record high $G_{m,ext}$ of ~870 μS/μm and the best quality factor *Q* of ~ 9.1 among all reported GeSn-based pMOSFETs.

To achieve high performance GeSn/Ge nMOSFETs, great challenges e.g. strong Fermi level E_F pinning, a large D_{it}, need to be addressed. In this context, vertical Ge/$Ge_{0.95}Sn_{0.05}$/Ge GAA nanowire nMOSFETs are fabricated and characterized. GeSn-channel nanowire nMOSFETs with decent electrical performance outperform Ge control devices, which emphasizes the advantage of high-mobility GeSn as the channel. With the performance-symmetrical Ge/$Ge_{0.95}Sn_{0.05}$/Ge nanowire nMOSFETs and $Ge_{0.92}Sn_{0.08}$/Ge nanowire pMOSFETs, the first proof of concept for a GeSn-based hybrid CMOS inverter is realized with a high voltage gain of ~18 at V_{DD}=0.8V. All in all, the vertical nanowire architecture along with Ge(Sn) material could potentially enable CMOS applications beyond 5 nm nodes.

Zusammenfassung

Während des letzten halben Jahrhunderts war die Miniaturisierung von Transistoren die Hauptantriebskraft für die Verbesserung der Leistungserzeugung von komplementären Silizium (Si)-Metall-Oxid-Halbleitern (CMOS) von Generation zu Generation im Hinblick auf die Verringerung der Gate-Länge, Gate-Breite und Oxiddicke, die als Moore'sches Gesetz bezeichnet wird. Die kontinuierliche Weiterentwicklung herkömmlicher planarer Bauelemente stößt jedoch aufgrund von verringerter Verlustleistung, Packungsdichte, elektrostatischer Steuerbarkeit und Variabilität an ihre Grenzen. Um den CMOS-Strategieplan zu erweitern, werden Ansätze zur Verwendung alternativer Kanalmaterialien und neuer Bauelementarchitekturen untersucht. Geramium (Ge) und neu entdeckte Germanium-Zinn (GeSn)-Halbleiter sind vielversprechende Materialien, da sie eine hohe Ladungsträgermobilität, eine kleine und abstimmbare Bandlücke besitzen und eine einfache Integration in die Si-Technologie ermöglichen. Darüber hinaus fand eine Entwicklung der Transistorarchitektur von der konventionellen planaren Struktur zu 3D-FinFETs und schließlich zu Gate-All-Around (GAA)-Nanodraht-Bauelementen statt, was zu einer überlegenen Gate-Elektrostatik und einer guten Immunität gegen Kurzkanaleffekte führt. Wie theoretisch vorhergesagt wird, bieten vertikale GAA-Nanodraht-Transistoren im Vergleich zu FinFETs und horizontalen Nanodraht-Transistoren, die als die ultimative Struktur für die klassische CMOS-Skalierung angesehen werden, weitere Skalierbarkeit, mehr Layout-Effizienz und weniger Stromverbrauch.

In dieser Arbeit wird die Anwendung von vertikalen Nanodrähten basierend auf GeSn/Ge in p-Typ- und n-Typ-MOSFETs untersucht und deren Einsatz elektrischen Schaltungen bewertet. In diesem Zusammenhang werden die wichtigsten Prozessmodule untersucht: (i) ein optimiertes Verfahren zum vertikalen Ätzen von Nanodrähten für ausgezeichnete Vertikalität d.h. glatte Seitenwände von Nanodrähte mit einem Durchmesser unter 20 nm werden durch digitales Ätzen erreicht, ähnlich wie beim Ätzen von Atomschichten; (ii) dielektrische Schichtstapel mit Nach-Oxidationspassivierung werden verwendet, um die Defektdichte an der Grenzfläche (D_{it}) zwischen Dielektrikum und Kanal zu reduzieren; (iii) für leistungsstarke MOSFETs werden ohmsche Kontakte sowohl für p- als auch n-Typ Ge(Sn) verwendet.

Vertikale Ge GAA-Nanodraht-pMOSFETs mit einem Top-Down-Ansatz werden zum ersten Mal experimentell demonstriert, die ausgezeichnete Unterschwellen-Eigenschaften aufweisen. Die Überlegenheit der elektrostatischen Integrität des Gates wird durch die Abhängigkeit der elektrischen Leistung von der Skalierung des Nanodraht-Durchmessers

bestätigt. Der Metallkontakt an der Nanodrahtspitze erweist sich als eine Herausforderung für vertikale Nanodraht-Transistoren. Aus dem Leistungsvergleich durch Vertauschen von Source und Drain ist sichtbar, dass der Deaktivierungseffekt der Dotierung in dünnen Nanodrähten für die Leistungsasymmetrie verantwortlich ist. Darüber hinaus zeigt die I-U-Charakterisierung bei niedrigen Temperaturen eine typische Temperaturabhängigkeit des Unterschwellenhubs (*SS*). Diese Abweichung zwischen den experimentellen Daten und dem idealen *SS* liegt hauptsächlich im D_{it} und dem Quellwiderstand. Die Schwellenspannung weist eine lineare Abhängigkeit von der Temperatur von 1,6 mV/K und 3 mV/K für 45 nm und 65 nm dicken Nanodraht-pMOSFETs.

Um eine verbesserte Leistung im eingeschalteten Zustand zu erzielen, werden $Ge_{0,92}Sn_{0,08}$/Ge GAA-Nanodraht-pMOSFETs durch Aufwachsen von GeSn auf der oberen Schicht hergestellt, um den spezifischen Kontaktwiderstand zu verringern. Berechnung der Verspannungsverteilung und Bandstruktur an der GeSn/Ge-Grenzfläche im Quasi-1D-Nanodraht zeigen Vorteile für die elektrischen Leistungskennzahlen. Mit einem skalierten EOT von ~2 nm erreichen GeSn/Ge-Nanodraht-pMOSFETs einen niedrigen SS von 67 mV/dec, einen Rekordwert für hohe $G_{m,ext}$ von ~870 µS/µm und den besten Qualitätsfaktor Q von ~ 9,1 GeSn-basierten pMOSFETs, der in der Literatur bekannt ist.

Um GeSn/Ge nMOSFETs herzustellen, müssen große Herausforderungen, z.B. starkes Fermi-Niveau E_F-Pinning oder eine hohe D_{it}, überwunden werden. In diesem Zusammenhang werden vertikale Ge/$Ge_{0,95}Sn_{0,05}$/Ge GAA-Nanodraht-nMOSFETs hergestellt und charakterisiert. GeSn-Kanal-Nanodraht-NMOSFETs mit guter elektrischer Leistung übertreffen Ge Bauteile, was den Vorteil der hoch beweglichen Ladungsträgern des GeSn als Kanal beweist. Mit den leistungssymmetrischen Ge/$Ge_{0,95}Sn_{0,05}$/Ge-Nanodraht-nMOSFETs und $Ge_{0,92}Sn_{0,08}$/Ge-Nanodraht-pMOSFETs wird der erste Proof-of-Concept für einen GeSn-basierten Hybrid-CMOS-Inverter mit einer hohen Spannungsverstärkung von ~18 bei V_{DD}=0,8V realisiert. Alles in allem könnte die vertikale Nanodraht-Architektur zusammen mit Ge(Sn) als Material potenziell CMOS-Anwendungen jenseits von 5 nm-Knoten ermöglichen.

Contents

List of Abbreviations

PPAC	Performance, power, Area and Cost
FEOL	Front-End-Of-Line
BEOL	Back-End-Of-Line
DIBL	Drain-Induced Barrier Lowering
SS	Subthreshold swing
CMOS	Complementary Metal–Oxide–Semiconductor
GAA	Gate-All-Around
IRDS	International Roadmap for Devices and Systems
FOMs	Figures Of Merits
NiGeSn	Nickelstanogermanide
R_{tot}	Total Resistance
G_{max}	Maximum transconductance
EOT	Equivalent Oxide Thickness
Q	Quality Factor
IC	Integrated Circuit
V_{DD}	Supply Voltage
V_{TH}	Threshold voltage
I_{OFF}	Off-State Current
I_{ON}	On-State Current
CGP	Contacted Gate Pitch
L_G	Gate Length
TEM	transmission electron microscopy

DTCO	Design-Technology Co-Optimization
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
C	Capacitance
SRAM	Static Random Access Memory
CPU	Central Processing Unit
VLS	Vapor-Liquid-Solid
SAE	Selective Area Epitaxial
EBL	Electron Beam Lithography
RIE	Reactive Ion Eetching
D_{it}	Density of Interface Traps
RIE	Reactive Ion Etching
HH, LH	Heavy Hole, Light Hole
FGA	Forming Gas Annealing
BTBT	Band-To-Band Tunneling
CVD	Chemical Vapor Deposition
HSQ	Hydrogen SylsesQuioxane
SEM	Scanning imaging microscopy
HCl	Hydrochloric Acid
HF	Hydrofluoric Acid
AFM	Atomic Force Microscope
ALE	Atomic Layer Etching
ALD	Atomic Layer Deposition
IL	Interfacial Layer
TEMAH	Tetrakis (ethylmethylamino) Hafnium

EDX	Energy-dispersive X-ray Spectroscopy
$\boldsymbol{\Phi_B}$	Schottky Barrier Height
CNL	Charge Neutrality Level
TLM	Transmission Line Method
ECV	Electrochemical Capacitance-Voltage
TCD	Top-Contact as the Drain
TCS	Top-Contact as the Source
GIDL	Gate-Induced Drain Leakage
TCAD	Technology Computer-Aided Design
SOI	Silicon-On-Insulator
RBS	Rutherford Backscattering Spectrometry
TOF-SIMS	Time Of Flight Secondary Ion Mass Spectroscopy
NEGF	Non-Equilibrium Green's Function
TNL	Trap Neutrality Level
NM	Noise Margin

List of Symbols

Symbol	Unit	Description
C	F	Capacitance
C_d	F, μF/cm^2	Depletion capacitance
C_{ox}	F, μF/cm^2	Oxide capacitance
C_{it}	F, μF/cm^2	Interface trap capacitance
D_{it}	cm^{-2}eV^{-1}	Density of interface charge
E	V/m	Electric field
E_C	eV	Conduction band energy
E_V	eV	Valence band energy
E_F	eV	Fermi energy
E_g	eV	Bandgap
h	Js, eVs	Planck constant
I_{DS}	A, μA/μm	Drain current
I_{OFF}	A, μA/μm	Off-state current
I_{ON}	A, μA/μm	On-State current
k_B	J/K, eV/K	Boltzmann constant
m^*	kg	Effective mass
n	cm^{-3}	n-type carrier concentration
N_A	cm^{-3}	Acceptor concentration
N_D	cm^{-3}	Donor concentration
q	C	Electric charge
R	Ω	Resistance
R_s, R_D	Ω	Source resistance, Drain resistance
R_{tot}	Ω	Total resistance
SS	mV/dec	Subthreshold swing

t	m	Thickness
T	K	Temperature
V	V	Voltage
V_{DS}	V	Drain voltage
V_{GS}	V	Gate voltage
ε	V/cm	Dielectric constant
μ	cm^2/V-s	Carrier mobility
κ	-	Relative permittivity
D	m, nm	Nanowire diameter
ρ_C	Ω·cm^2	Contact resistivity
R_{SH}	Ω/	Sheet resistance
$G_{m,ext}$	μS/μm	Extrinsic transconductance
DIBL	mV/V	Drain-induced barrier lowering
r	m, nm	Radius

1. Introduction

According to a new forecast from International Data Corporation (IDC), worldwide spending on information and communications technology (ICT) will be $4.3 trillion in 2020, an increase of 3.6% over 2019, particularly due to the booming applications of big data, mobility, and cloud (Internet of Things and servers) [1]. The evolution of diversification and omnipresence in ICT has enabled tremendous convenience and benefit of modern society, meanwhile, enormous challenges for the power efficiency have become the most important issues. Great efforts have made to propose low power schemes while providing comparable performance for specific devices, especially in semiconductor industry. Device miniaturization straightforwardly by dimensional scaling is the main driver to gain benefit in the semiconductor field, which is ramped into manufacturing on approximately a two year cadence, known as Moore's Law [2]. At each technology node, which represents the progression of device scaling, the improvement of microchip performance, power, area and cost (PPAC) is expected. PPAC scaling is aimed at to enhance circuit performance by 30%, decrease the power consumption by 50%, reduce the chip area by 50%, and lower the wafer cost by 30% without degradation in reliability [3-4]. With no physical meaning to particular feature sizes, current technology node name is adopted to reflect the 70% dimension scaling necessary to double transistor density and typically refers to the recent 22 nm, 14 nm, 10 nm, 7 nm etc. At the time of this writing, the most advanced technology node in high-volume production is the 7 nm node [5], with the 5 nm node in advanced development [6] and 3 nm node in early exploration [7].

Currently at 7 nm node, the transistor gate length is shrank incredibly to 15 nm, approaching physical limitation [5]. Apparently, the aggressive scaling targets in the following nodes are difficult to maintain with new problems arising. The scaling challenges call for significant innovations including but not limited to front-end-of-line (FEOL) at the transistor level, e.g. suppressing short channel effects, and interconnect with wiring on the chip, e.g. reducing RC delay, referred to back-end-of-line (BEOL). Semiconductor material innovation towards high-mobility channel has been one promising option to maintain high performance and low power targets for microchips, including group III-V [8-9], two-dimensional (2D) materials [10-12], and group IV materials [13-14]. Group III-V, such as InGaAs with superior electron transport properties is viable for n-type transistors, nevertheless, its unsatisfactory p-type counterpart along with the incompatible integration on Si wafers lead to difficulties for

industrial manufacturing. 2D materials, e.g. MoS_2, with atomically thin body, dangling bond-free surface and high mobilities, bring unique features to transistors. However, there are many challenges facing 2D nanoelelectroncis, such as large-scale high-quality synthesis and contact resistance issues. As a contrast, SiGeSn-based group IV materials, the focus of this work, are highly promising due to excellent carrier transport, tunable bandgap and easy integration on Si wafers etc. So far, state-of-the-art planar transistors and FinFETs have been already achieved with main-stream manufacturing based on Si and SiGe in the industry. In this regard, more investigations on SiGeSn alloys should be exploited to potentially extend Moore's Law in the future nodes.

More recently, the industry has witnessed the migration of transistor architecture from conventional planar structure to non-planar 3D FinFET from 22 nm node [15]. A conducting fin-like channel rises above the planar surface of the wafer, which is wrapped around by tri-gates. The 3D structure necessitates superior gate electrostatic control over the channel and therefore owns better immunity against short-channel effects, e.g. suppressing drain-induced barrier lowering (DIBL), lowering the high leakage current and improving subthreshold swing (*SS*). In addition, FinFETs can deliver higher current drive per footprint compared with planar transistors. However, while following the rigid scaling scenarios, FinFETs cannot afford the continuation of advantages after 5 nm node [6-7]. As a successor of FinFETs, gate-all-around (GAA) nanowire transistors have been proposed for the following nodes due to the ideal electrostatic controllability via fully surrounding gate, which is considered as the ultimate structure for the classical complementary metal–oxide–semiconductor (CMOS) roadmap [16-18].

For the first time, the proposal and demonstration of GAA nanowire transistor concept on Si dated back to 1988 [19] and later on, numerous research has been done using different material systems and approaches. The GAA nanowire schemes can be categorized into horizontal (already under exploration by the industries) and vertical. Due to the complexity of transistor processing, chips based on horizontal GAA nanowire transistor will be in main-stream manufacturing after 2022 [20], while vertical GAA nanowire will be essentially implemented even later predicted by the International Roadmap for Devices and Systems (IRDS) [3]. According to performance evaluation in circuit-level modeling, GAA nanowire transistors with a vertical architecture can deliver further scalability, more layout efficiency and less power consumption compared to FinFETs and horizontal GAA nanowire devices [21-22]. What is more, vertical nanowire devices can relax lithography limitations by decoupling footprint scaling from gate length and contact placement scaling, since the achievable gate length is determined by the planarized thin film technology instead.

In the framework of this thesis, the properties of vertical GAA nanowire CMOS transistors based on Ge(Sn) semiconductors are investigated and the prospects for future low power and high performance logic applications are examined. The thesis is organized in the following way. To start with, in chapter 2, background of power-constrained scaling is introduced, followed by the scaling roadmaps from planar transistors to FinFETs and ultimately GAA nanowire transistors. Lastly, as the main body of this thesis, vertical GAA nanowire transistors based on Ge(Sn) semiconductors are highlighted.

The key process modules for vertical GAA nanowire platform are investigated in chapter 3. Literature review for each module is given, followed by a detailed discussion of our well-developed fabrication techniques, e.g. nanowire patterning, surface passivation, planarization. After those critical modules are optimized, this vertical nanowire platform is applied for the experimental parts of this thesis and moreover, this platform can also be transferred to various SiGeSn heterostructures and device applications, e.g. tunneling transistors, photonic devices.

The device fabrication and electrical characterization of Ge(Sn)-based vertical GAA nanowire pMOSFETs are studied in chapter 4. Thanks to optimized dry etching, post-oxidation passivation and NiGe metallization, high performance Ge GAA nanowire pFETs show low *SS* of 66 mV/dec, small *DIBL* and I_{ON}/I_{OFF} ratios of > 10^6. The systematical study of nanowire diameter scaling on key electrical figures of merits (FOMs) is investigated. It follows the classical diameter scaling principles except the smallest nanowire devices. The gate electrostatics for the GAA nanowire devices are also confirmed. I_{ON}, R_{tot} and G_{max} asymmetry is attributed to the doping deactivation effect in small nanowires. Low temperature dependence study shows that robust surface passivation and contacts in vertical nanowire transistors should be developed.

From what is obtained from Ge nanowire pFETs study, it's found that top contact resistance is the key bottleneck for vertical nanowire devices. Therefore an introduction of top GeSn layers leads to the following GeSn/Ge heterostructure nanowire pFETs. Electrical performance comparisons between devices with and without NiGeSn metallization are conducted. The devices with NiGeSn metallization show improved performance in terms of R_{tot}, G_{max}, *DIBL* compared to Ge control devices. The influence of nanowire diameter scaling and equivalent oxide thickness (EOT) scaling on the electrical characteristics is analyzed. The GeSn/Ge nanowire pFETs with EOT =2 nm demonstrate low *SS* of 67 mV/dec, highest $G_{m,ext}$ of 870 µS/µm and record high quality factor *Q* of 9.1 among reported GeSn-based pFETs.

Furthermore, Ge(Sn)-based nanowire nFETs as an indispensable counterpart for CMOS circuits are studied in chapter 5. Based on Ge n^+-n^--n^+ and Ge/$Ge_{0.95}Sn_{0.05}$/Ge n^+-n^--n^+ material

stacks, Ge(Sn)-based vertical nanowire nMOSFETs are fabricated and characterized, which emphasizes the advantage of high-mobility of GeSn channel. Subsequently, CMOS inverters built from p-type and n-type transistors are conducted. The voltage transfer characteristics of an inverter is discussed and the further improvement is pointed out. At last, a summary is given in chapter 6. The prospects of Ge(Sn)-based vertical GAA nanowire transistor are considered in an outlook.

2. Background and physics of GAA nanowire transistors

Contents

In this chapter, the background and fundamental principles of GAA nanowire transistors aimed at CMOS scaling are studied and evaluated. A review of power-constrained scaling as well as Moore's Law is given. The scaling of CMOS roadmap consists of the transistor architecture evolution from planar, to FinFETs and ultimately GAA nanowire structures. The necessity of GAA nanowire transistors is extensively discussed. A special emphasis is laid on the adoption of vertical GAA nanowire transistors for the sub-5 nm nodes, which is the focus of this thesis. Vertical GAA nanowire architecture can outperform horizontal GAA one in terms of the device layout area, switching speed, and power consumption. Detailed discussions in the device level, layout, and power consumption in the circuit level are systematically investigated. Finally, to satisfy high performance and low power targets, non-silicon high mobility semiconductors are imperative. Ge(Sn) with high carrier mobility, easy application of strain engineering and bandgap engineering, and compatibility with Si-based

processing is beneficial to replace Si channel. Combining new device architecture and novel materials could achieve ultimately scaled CMOS devices and provide a viable path to further extend Moore's Law.

2.1. Power consumption in energy-efficient chips

The development of information and communications technology features the unrelenting, always accelerating change. Applications based on ICT have acquired a strong foothold in everyday life, e.g. high-performance computing, artificial intelligence (AI), and 5G communications. For example, the wide availability of Internet access including cellphones, laptops shapes the way how we communicate with each other and how we deal with the massive data. The continuous semiconductor technology revolution has been driven by those application landscapes and is still ongoing. Significant innovation and breakthrough by the industry and academia have been made in the past half a century. For example, in 1958, the first integrated circuit (IC) was invented by Jack Kilby at Texas Instruments, which laid the foundation of very-large-scale-integration circuits (VLSI) [23]. The first commercial single-chip microprocessor, the Intel 4004, was released in 1971 [24]. Flash memory, invented by Fujio Masuoka led to low-cost, high-capacity memory in diverse electronic products [25].

Yet, especially recently, these key technologies which have fueled the advanced growth of the semiconductor industry seem to encounter a wall dictated by physical limitations, creating serious technological challenges for computing power and communication speed. For example, the data centers in the United States consumed about 70 billion kilowatt-hours of energy, accounting for 1.8% of all the energy consumption in 2016 and up to 3% nowadays [26]. Therefore, to fulfill the adequate performance requirement and keep energy efficiency, device innovations should be fundamentally explored.

2.1.1 Power-constrained scaling

The transistor evolution also follows another famous scaling rules: Dennard scaling, proposed by R. H. Dennard in 1974 [27]. The rules are summarized in table 2.1. It holds the principle of constant-field scaling, which is that device dimensions and device voltages are scaled such that electric fields (both horizontal and vertical) remain essentially constant. To ensure that the reliability of the scaled device is not compromised, the electric fields in the scaled device must not increase. Typically, the scaling factor $k \approx 0.7$ per technology generation. This means transistor dimensions could be scaled by 30% (0.7x), thus reducing their area by 50% and circuit delays by 30% (0.7x). To keep the electric field constant, the voltage is also reduced

by 30%, leading to power reduction by 50% and constant power density. Historically from 1958 to 2006, Dennard scaling allows semiconductor manufacturers to drastically decrease the energy consumption by about 5 orders of magnitude and increase the number of transistors in a chip by 9 orders of magnitude.

Table 2.1 Transistor scaling scenario and parameters

	Device and circuit parameters	Scaling factor (k <1)
Scaled parameters	Device dimensions (L_G, W, t_{ox})	k
	Doping concentration (N_a, N_d)	$1/k$
	Voltages V	k
Effect on device parameters	Electric field E	1
	Capacitance ($C=\epsilon A/t$)	k
	Drift current I	k
Effect on circuit parameters	Device density	$1/k^2$
	Power density	1
	Power dissipation per device ($P = IV$)	k^2
	Circuit delay time (CV/I)	k

Here L_G is the gate length, W the gate width, t_{ox} the dielectric thickness, N_a the acceptor concentration, N_d the donor concentration, ϵ the dielectric constant, and A the device area.

However, the golden age of scaling appears to be broken down at 0.13 μm technology node in 2006. The power density by logic chips even hit an incredible 100 $W.cm^{-2}$, resulting in unpractical cost for associated packaging and cooling peripheral for a microprocessor. The fundamental reason cited for the breakdown is at scaled dimensions, the leakage current I_{OFF} poses great challenges and causes the chip to heat up.

In the typical I_D-V_G transfer characteristics for transistors as shown in Fig. 2.1 [28], improved performance needs the supply voltage V_{DD} and simultaneously the threshold voltage V_T to be scaled since on-state current I_{ON} is proportional to $(V_{DD}-V_T)^2$. However, continuous V_T down-

scaling leads to an exponentially increase of I_{OFF}, as indicated by the vertical intercept of *I-V* curves. Because I_{OFF} has a strong dependence on V_{TH} described by the following [29]:

$$I_{OFF} \approx a\frac{1}{L}\exp(\frac{q(V_G - V_T)}{kT} \tag{2.1}$$

Where *a* is a constant, *k* the Boltzmann constant, and *T* the operation temperature.

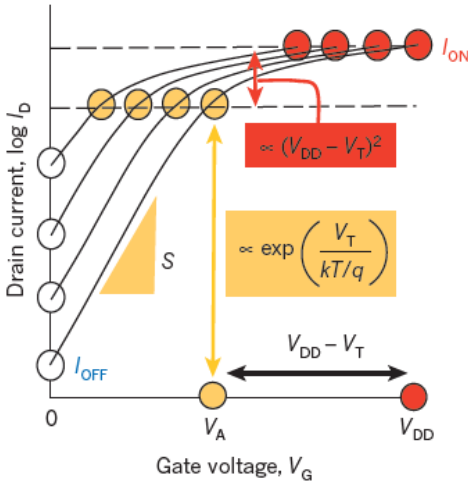

Fig. 2.1 Typical I_D-V_G transfer characteristics of a MOSFET illustrating an exponential increase in I_{OFF} due to the scaling of V_T while simultaneous scaling of V_{DD} and V_T to keep the gate overdrive V_{DD}-V_T for comparable I_{ON}, reproduced from [28].

The unsustainable I_{OFF} scaling is fundamentally due to the non-scalability of *SS*, which cannot be reduced below 60 mV/decade. *SS* is denoted as the steepness of the switching, which can be calculated by [30]:

$$SS = \frac{\partial V_G}{\partial log I_D} = \frac{dV_G}{d\Phi_s}\frac{d\Phi_s}{dlogI_D} \cong \left(1 + \frac{C_d + C_{it}}{C_{ox}}\right)(\ln 10)\frac{kT}{q} \tag{2.2}$$

Where V_G and Φ_S are the gate voltage and surface potential, I_D the drain current, C_d, C_{it} and C_{ox} the depletion capacitance, interface traps capacitance and oxide capacitance, respectively. In the ideal case, *SS* is approximately (ln10)*kT*/*q*= 60 mV/decade at room temperature. This means the transistor requires at least 60 mV of gate voltage to increase the drain current by one order of magnitude at room temperature.

The total switching energy for a logic operation can be written with the dynamic term $E_{dynamic}$ and the leakage term $E_{leakage}$ as follows [28]:

$$E_{tot} = E_{dynamic} + E_{leakage} = \alpha C_L {V_{DD}}^2 + V_{DD} I_{off} t_{delay} \tag{2.3}$$

Here α is an activity factor given by the average number of transitions on a node per clock cycle, C_L the total load capacitance, and t_{delay} the circuit delay time.

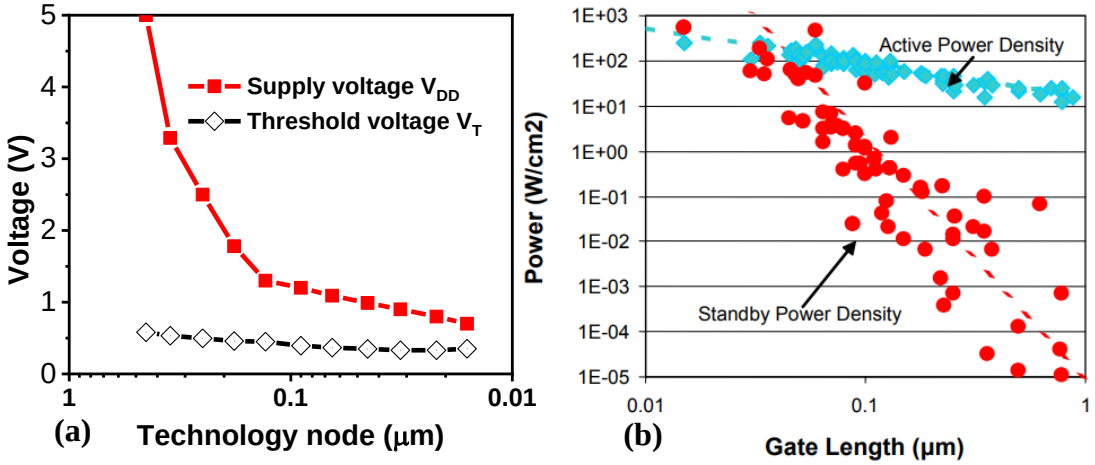

Fig. 2.2(a) Supply voltage V_{DD} and threshold voltage V_T scaling trends as a function of technology nodes based on IRDS [3]. V_{DD} scales faster than V_T, while V_T is scaled more gradually over the technology nodes. (b) Power dissipation trend including active power and standby power in integrated circuits with gate length scaling. As the gate length shrinks below 32 nm node, the leakage power starts to dominate the total power consumption due to the growth of I_{OFF}. It is getting impossible to have both desired dynamic and leakage power targets in advanced technology nodes, reproduced from [31].

From equation (2.3), scaling V_{DD} and I_{OFF} can result in the reduction of dynamic and leakage power consumption. Meanwhile, it also requires the V_T scaling in proportion to the gate length at each node. However, from the V_{DD} and V_T scaling trends as a function of technology nodes in Fig. 2.2 (a), the supply voltage V_{DD} scales faster than V_T, while V_T is scaled more gradually. This is because I_{OFF} increases exponentially when V_T decreases (see equation (2.1)). Therefore, the leakage power consumption will also increase with nodes scaling, which sets a lower limit to the scaling down of V_T. Consequently, the scaling of V_{DD} out-of-proportion to V_T reduces I_{ON} and also switching speed. As the gate length shrinks below 32 nm node, the leakage power starts to dominate the total power consumption as shown in Fig. 2.2 (b). It is getting impossible to have both desired dynamic and leakage power targets in advanced technology nodes. To address this problem, multiple V_T assignments are developed to enable design flexibility for power and performance trade-off in modern chips. In the high-performance applications, V_T is set to be low, keeping gate overdrive higher and thus higher I_{ON} and switching speed, however, it is at the cost of substantially higher leakage current and power consumption. On the contrary, for low power targets, V_T is aimed high, therefore decreasing the leakage power.

With the breakdown of Dennard scaling, transistor scaling has already stepped into an era of power-constrained scaling. Nowadays, the microprocessors cannot maintain increasing clock frequency while keeping power density the same, instead the manufacturers turn to multicore processors to improve performance, however, it cannot fundamentally solve the increasing power dissipation issues [32]. To continue Moore's Law for low power, high performance requirements, it is imperative to explore potential solutions based on channel materials and transistor architectures. In the next section, we will review the scaling process of the CMOS roadmap.

2.2. Scaling of CMOS roadmap

When it comes to Moore's Law, specifically, it is proposed by Gordon Moore in 1965 [2], revealing an empirical relationship that the transistor counts in an integrated circuit double about every two years. This prediction has been followed by the semiconductor industry and sets the targets for transistor development for more than 5 decades. The transistor counts were at the order of thousands at the beginning and ramp up to billions currently, witnessing the enormous progress of Moore's Law [33]. The geometrical scaling of transistors also leads to the simultaneous improvement of PPAC at each technology node. What is more, the development of the microelectronic field, such as the improvement of memory, sensor, radio-frequency applications, has strongly linked to Moore's Law. The technological advancement has been a driving force for economic growth and social productivity.

From the point of view of a basic transistor unit, the geometrical scaling includes the scaling of contacted gate pitch (*CGP*), gate length (L_G), gate width (W) and dielectric thickness (t_{ox}), as is discussed by Dennard scaling. Fig. 2.3 (a-b) show the cross-sectional schematic and a corresponding transmission electron microscopy (TEM) image of a typical transistor. Simultaneous dimensional scaling has been continued with also PPAC improvement until degradation issues occur at 90 nm technology node, such as short-channel effects, increased leakage power. Moreover, the parasitic effects, e.g. capacitive coupling and series resistance in interconnect cannot be neglected. Simply feature size scaling technology cannot fulfill the tradeoff between performance and power targets, and urgently requires innovative knobs to extend the scaling. Innovative ways to further extend Moore's Law have been continuously sought [35]. For example, at 90 nm node, strain engineering was proposed to enhance the carrier mobility [36]. At 45 nm node, high-κ/metal gate (HKMG) technology was introduced in commercial products [37]. The main advantages of HKMG are the drastic reduction in gate leakage current and the associated possibility of further scaling.

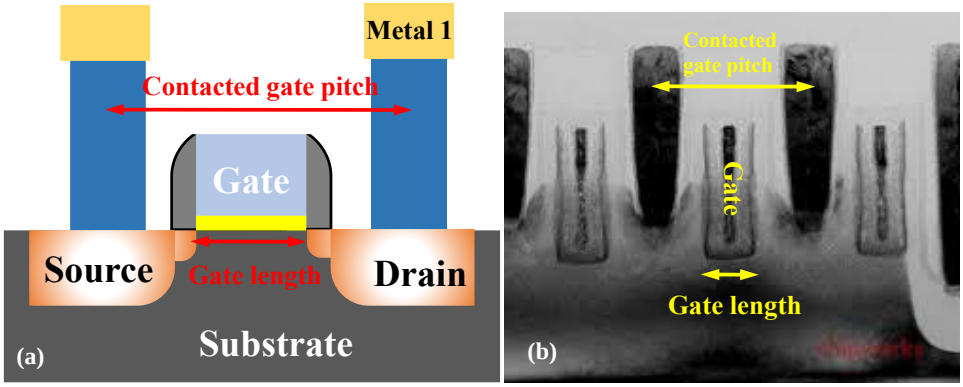

Fig. 2.3 (a) Cross-sectional schematic of a transistor, featuring source, drain, gate and metal 1. The geometrical scaling includes the scaling of contacted gate pitch (*CGP*), gate length (L_G), gate width (W), dielectric thickness (t_{ox}) and spacer thickness, as is discussed by Dennard scaling. (b) Cross-sectional TEM image of TSMC 16-nm transistors, which as a comparison, corresponds to the schematic in (a), reproduced from [34].

Continuous scaling using a planar transistor structure cannot provide enough gate electrostatic control over the shorter channel. In 2011, Intel was the first company to propose an unprecedented 3D tri-gate transistor (known as FinFETs) for high-volume manufacturing [38]. The tri-gate transistor has a rather thin fin channel that rises vertically. A gate wraps around three sides of the fin with stronger gate electrostatics. This means more current drive when it is in the on-state regime while lower leakage current during the off-state regime. Moreover, multiple fins can be added together to increase the drive strength for high-performance applications. In short, the 3D transistors enable microchips to operate at lower voltage with lower leakage, providing a novel combination of improved power savings and performance gains compared to previous state-of-the-art planartransistors. For example, the 22 nm tri-gate transistors are 18% and 37% faster at a supply voltage of 1V and 0.7 V, compared to Intel's 32 nm planar transistors [35].

The transition to 3D transistors continues the pace of technology advancement, fueling Moore's Law for years. As was illustrated in Fig. 2.3, in the basic transistor unit, the gate, sidewall spacers and source/drain compete for limited placement space within the CGP, resulting in difficulties of continuous scaling. Fig. 2.4 (a) shows the predicted first-order scaling trend of *CGP*, L_G, and spacer length for upcoming technology nodes [21]. The typical feature sizes continue to decrease to get the desired PPAC whereas L_G is reduced steadily to suppress short-channel effects. However, as following the scaling rules, at 3 nm node, the spacer width will be 0, which is impossible to cut the parasitic capacitance between the source/drain and gate contacts. Accordingly, the FinFET also has to shrink the fin width to keep good electrostatics. In Intel's 14 nm node, the fin width is only 8 nm in the middle of

the fin height (Fig. 2.4(b)). From the history of planar transistor scaling, dimensional scaling for FinFETs also encounters the same problems and cannot sustain scaling forever. In recent years, a joint design-technology co-optimization (DTCO) effort has focused on scaling boosters for FinFETs, such as self-aligned gate contacts, buried power rails, high mobility channels [40-41].

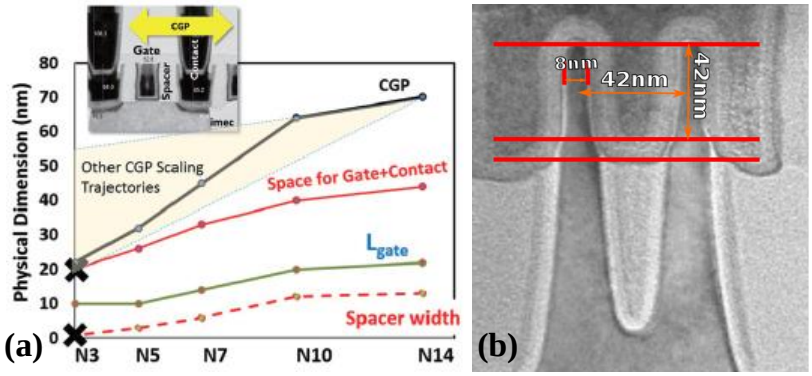

Fig. 2.4 (a) the predicted first-order scaling trend of *CGP*, L_G, and spacer length for upcoming technology nodes. The typical feature size continues to decrease to get the desired PPAC whereas L_G is reduced steadily reproduced from [21]. (b) The TEM image of a fin in Intel's 14 nm technology node. The fin width is only 8 nm in the middle of the fin height, reproduced from [39].

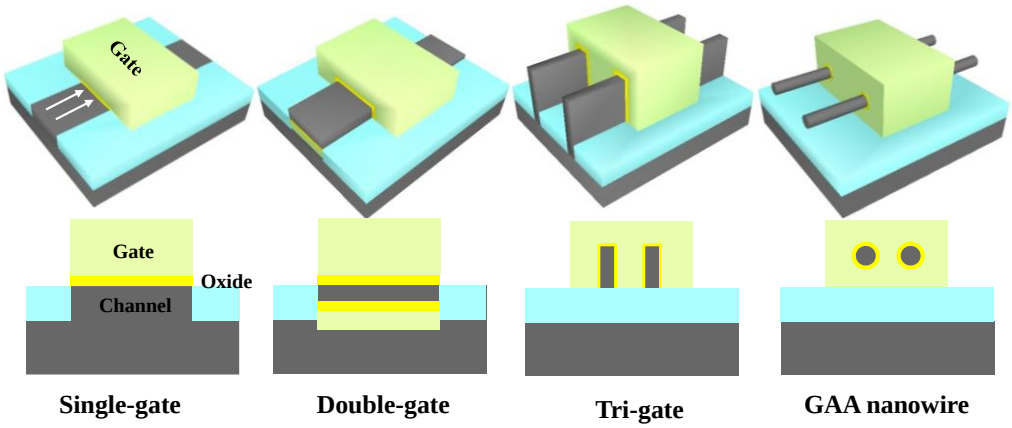

Fig. 2.5 The evolution of transistor architecture from planar to Fin, and ultimately to GAA structures (i.e. nanowire) and corresponding device cross-sections viewed in the current flow direction. They show the increasing gate electrostatic integrity over the channel as the gate numbers increase.

2.3. The necessity of GAA nanowire

As was mentioned earlier, FinFETs can deliver better electrostatic controllability than planar transistors, and finally lead to footprint scaling at 5 nm node with L_G < 12 nm [6]. However, for further nodes beyond sub-5 nm, FinFETs cannot provide enough gate electrostatic integrity to sustain the scaling. Extreme short-channel effects become critical issues again. Mitigating short-channel effects requires the transistor architecture evolution from planar to Fin, and ultimately to GAA structures (i.e. nanowire or nanosheet) as shown in Fig. 2.5. The surrounding gate control of the GAA transistor can provide ideal electrostatic integrity, which is considered as the end of the CMOS roadmap.

2.3.1 Natural length λ

The advantage of the GAA structure can be characterized by natural length λ (also referred to as screening length). λ, physically represents the penetration of the drain electric potential on the surface potential in the channel, as electrical fields of the drain and gate compete for the controllability. Generally, a small λ is desired to mitigate short-channel effects. To put it simply, this effect can be understood by the surface potential Φ_s comparison along the channel for the long-channel and short-channel MOSFETs as illustrated in Fig. 2.6. As the drain bias increases, the conduction band is pulled down, leading to the expansion in the drain-channel depleted region as shown in Fig. 2.6 (a). In the long-channel devices, the drain potential does not have an apparent impact on the source-channel potential barrier, as indicated by λ. When scaling down the channel length, the depletion regions between source-channel and drain-channel become coupled (Fig. 2.6 (b)). The drain potential has a strong effect on the potential bending over the source-channel region, leaving only a fraction of charge controlled by the gate. This gives rise to the DIBL effect, which can be approximated using the following [42-43]:

$$DIBL = 0.80 \cdot \frac{\varepsilon_{Si}}{\varepsilon_{ox}} \cdot \left[1 + \frac{x_j^2}{L_{el}^2}\right] \cdot \frac{t_{ox}}{L_{el}} \cdot \frac{t_{dep}}{L_{el}} \cdot V_d = 0.80 \cdot \frac{\varepsilon_{Si}}{\varepsilon_{ox}} \cdot V_d \cdot EI \tag{2.4}$$

Where ε_{Si} and ε_{ox} is the permittivity of Si and oxide. x_j denotes the junction extension depth, L_{el} is the electrical channel length and t_{dep} is the depletion depth in the channel underneath the gate. *EI* represents electrostatic integrity and depends on the device geometry.

DIBL effect results in a loss of electrostatic control, which has a strong dependence on applied V_d. As a consequence, simply applying the gate voltage V_g to turn off the transistor can be partially counteracted by V_d, hence leakage current flows even below threshold voltage V_{TH}.

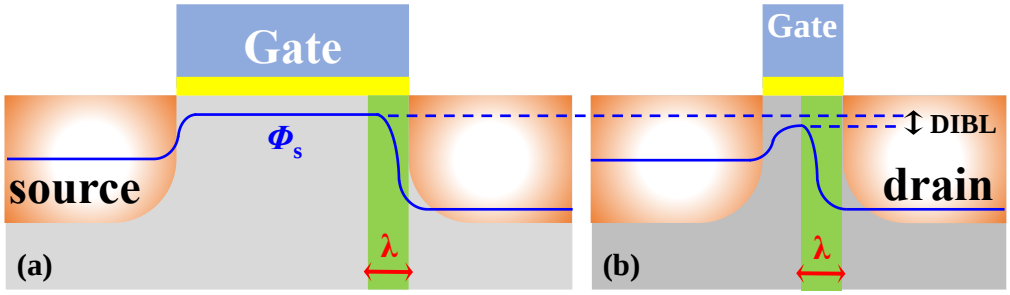

Fig. 2.6 (a) The effect of drain potential on the surface potential Φ_s along the channel for the long-channel and short-channel MOSFETs. As the drain bias increases, the conduction band is pulled down, leading to the expansion in the drain-channel depleted region. When scaling down the channel length, the depletion regions between source-channel and drain-channel become coupled.

Analytical expressions for λ are dependent on the device geometry, it can be calculated with corresponding boundary conditions for structures in Fig. 2.5. What is more, λ can be used to estimate the maximum Si body and gate oxide thickness to suppress short-channel effects. In this work, Ge-based GAA nanowire transistors are proposed and investigated in detail. Hence, the λ derivation with Ge GAA nanowire structure is specifically presented as follows:

To describe the electrostatics governing the channel, the electric potential of 3D transistors is determined by Poisson's equation [44]:

$$\frac{d^2\emptyset(x,y,z)}{d^2x}+\frac{d^2\emptyset(x,y,z)}{d^2y}+\frac{d^2\emptyset(x,y,z)}{d^2z}=\frac{qN_a}{\varepsilon_{Ge}} \tag{2.5}$$

Where N_a is the channel doping (assumed to be the case of uniform doping)

To better solve the equation, the cylindrical coordinate system is thus used:

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial}{\partial r}\emptyset(r,z)\right)+\frac{\partial^2}{\partial z^2}\emptyset(r,z)=\frac{qN_a}{\varepsilon_{Ge}} \tag{2.6}$$

Where r is the radius of the nanowire and z is the transport direction along the channel.

A parabolic potential solution is assumed according to Young [45]:

$$\emptyset(r,z)=c_0(z)+c_1(z)r+c_2(z)r^2 \tag{2.7}$$

By applying the three boundary conditions for equation 2.7 listed below.

1) The center potential $\emptyset_c$ is a function of z only.

$$\emptyset(0,z)=\emptyset_c(z)=c_0(z)$$

2) The electric field in the center of the Si nanowire is zero

$$\frac{d}{dr}\Phi(r,z)|_{r=0} = 0 = c_1(z)$$

3) The electric field at the Ge/oxide interface can be derived from the gate potential $\emptyset_{gs}$, the surface potential $\emptyset_s$ and Ge nanowire and oxide thickness (The ideal interface is assumed).

$$\frac{d}{dr}\emptyset(r,z)|_{r=\frac{t_{Ge}}{2}} = \frac{\varepsilon_{ox}}{\varepsilon_{Ge}}\left(\frac{\emptyset_{gs}-\emptyset_s(z)}{\frac{t_{Ge}}{2}\ln(1+\frac{2t_{ox}}{t_{Ge}})}\right) = t_{Ge}c_2(z)$$

The final solution for ∅(r,z) after applying the boundary conditions are:

$$\emptyset(r,z) = \emptyset_c(z) - \left(\frac{2\varepsilon_{ox}r^2(\emptyset_c(z)-\emptyset_{gs}}{\varepsilon_{Ge}t_{Ge}^2\ln\left(1+\frac{2t_{ox}}{t_{Ge}}\right)+\frac{\varepsilon_{Ge}t_{Ge}^2}{2}}\right) \tag{2.8}$$

At the nanowire center, $r = 0$, Poisson's equation can be solved:

$$\frac{\partial^2}{\partial z^2}\emptyset_c(z) - \frac{\emptyset_c(z)-\emptyset_{gs}}{\lambda^2} = \frac{qN_a}{\varepsilon_{Ge}} \tag{2.9}$$

Where λ is

$$\lambda = \sqrt{\frac{2\varepsilon_{Ge}t_{Ge}^2\ln\left(1+\frac{2t_{ox}}{t_{Ge}}\right)+\varepsilon_{ox}t_{Ge}^2}{16\varepsilon_{ox}}} \tag{2.10}$$

λ characterizes the length scale for channel potential variation. Similarly, λ can be derived for device structures with single-gate, double-gate, tri-gate, and GAA nanowire corresponding to Fig. 2.5 in Table 2.2. Compared with the transistors aforementioned with the same body and oxide thickness, GAA nanowire devices show the smallest λ, demonstrating the ideal electrostatics.

In order to obtain minimal short-channel effects, effective gate length L_g should be far larger than λ ($L_g >> \lambda$). Studies show that the effective gate length must be at least four times larger than λ to manage good performance [46]. To visualize the impact of λ with various gate structures on the electrical performance, e.g. DIBL effect, Fig. 2.7 shows DIBL as a function of the ratio of effective gate length and λ (L_{eff}/λ), With decreasing L_{eff}/λ and L_{eff}, DIBL for

all specified structures get deteriorated as expected, nevertheless, GAA nanowire devices show the smallest DIBL effect at a given effective gate length, demonstrating suppressed short-channel effects and less strict rules for dimensional scaling [47]. Therefore, sophisticated solutions of GAA nanowire architecture can be adopted to extend the CMOS roadmap.

Table 2.2 λ comparison for Ge-based single-gate, double-gate, tri-gate and GAA nanowire transistors

Geometry	Natural length λ
Single-gate	$\sqrt{\frac{\varepsilon_{Ge} t_{Ge} t_{ox}}{\varepsilon_{ox}}}$
Double-gate	$\sqrt{\frac{\varepsilon_{Ge} t_{Ge} t_{ox}}{2\varepsilon_{ox}}}$
Tri-gate	$\sqrt{\frac{\varepsilon_{Ge} t_{Ge} t_{ox}}{2(\varepsilon_{ox} t_{Ge} + \varepsilon_{Ge} t_{ox})}}$
GAA nanowire	$\sqrt{\frac{2\varepsilon_{Ge} t_{Ge}^2 \ln\left(1 + \frac{2t_{ox}}{t_{Ge}}\right) + \varepsilon_{ox} t_{Ge}^2}{16\varepsilon_{ox}}}$

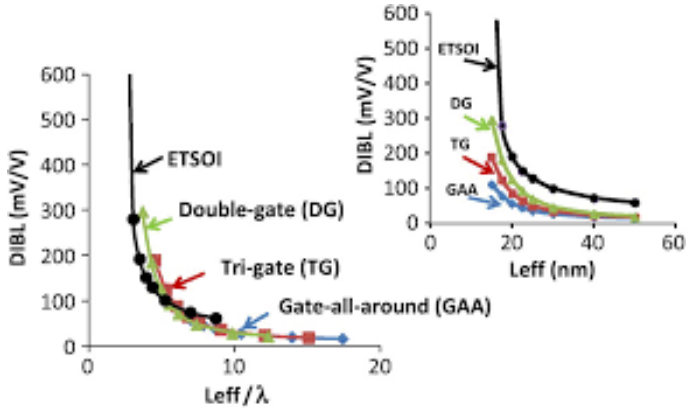

Fig. 2.7 DIBL as a function of the ratio of effective gate length and λ (L_{eff}/ λ), inset shows DIBL versus effective gate length. With decreasing L_{eff}/ λ and L_{eff}, DIBL for all specified structures get deteriorated as expected, nevertheless, GAA nanowire devices show the smallest DIBL effect at a given effective gate length, demonstrating suppressed short-channel effects and less strict rules for dimensional scaling, reproduced from [47].

2.4. The advantage of vertical GAA nanowire

The GAA nanowire patterning schemes can be horizontal or vertical. However, horizontal nanowire configuration, similar to FinFET still utilizes conventional 2D layouts, and unavoidably reaches physical limits by continuous scaling. For the ultimate CMOS architecture beyond 5 nm nodes, the vertical GAA nanowire approach can outperform horizontal GAA one in terms of the device layout area, switching speed and power consumption [21-22]. Comparisons among FinFET, horizontal nanowire and vertical nanowire transistors are given in this session. The discussions, e.g. parasitic resistance and capacitance in the device level, layout efficiency and power consumption in the circuit level are systematically investigated. To sum up, the vertical nanowire transistor will eventually lead to a paradigm shift in the device and circuit design, especially with the promotion of DTCO.

2.4.1. Ultimate vertical GAA nanowire transistor

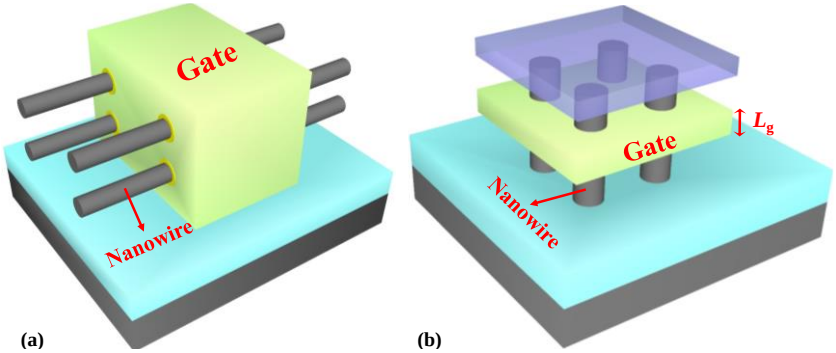

Fig. 2.8 3D schematic of (a) horizontal GAA nanowire transistor with vertically stacked nanowires, (b) vertical GAA nanowire device with vertical gate length definition. It moves from a 2D to 3D layout configuration, which decouples footprint scaling from CGP scaling due to the vertical placement.

In vertical GAA nanowire transistors, the current transport along the channel is aligned perpendicular to the planar surface. When combined with the superior gate electrostatic controllability by GAA geometry, a vertical nanowire transistor has been considered as a strong candidate to extend the CMOS roadmap. Vertical nanowire transistor, schematically shown in Fig. 2.8, moves from a 2D to 3D layout configuration with a fundamental change of vertical gate length definition. In planar, FinFETs or horizontal configurations, they still suffer from lithography limitations since there is not enough space within CGP, which was discussed in section 2.2. As a contrast, vertical nanowire design decouples footprint scaling from CGP scaling due to the vertical placement, thus providing a viable path to overcome the

gate-contact-CGP tyranny beyond sub-5 nm nodes. In this regard, the gate length determined by the thin film planarization can be more relaxed without the area penalty. This is an important knob for suppressed short-channel effects and improved transistor variability. Furthermore, it in turn allows nanowire diameter relaxation while keeping minimal short-channel effects. This is also beneficial for nanowire transistors with high-mobility alternatives, e.g. III-V and Ge, as mobility degradation below a certain nanowire diameter takes place due to quantum confinement or strong surface roughness, which would offset the gains of high-mobility materials [47].

Device parasitic resistance R and capacitance C among FinFETs, horizontal and vertical nanowire transistors are discussed analytically [22]. The dimensions and doping parameters are chosen aimed at the projected 5 nm node. From parasitic R values comparison in Fig. 2.9 (a), a vertical nanowire device shows the lowest resistance compared to other device architectures. It is noted that for the vertical nanowire structure shown here, source resistance R_S (including series and contact resistance) is not equal to drain resistance R_D. The resistance asymmetry is due to the contact path difference. As a result, R_S/R_D asymmetry has to be taken into account in circuit design. Further discussion will be conducted in Chapter 4. Besides, the parasitic C values as shown in Fig. 2.9 (b) can also confirm the advantage of vertical nanowire architecture. Gate-to-source and gate-to-drain capacitance (C_{GD}, C_{GS}) exhibit lowest due to the vertical placement of insulators among gate, source and drain. From the benchmark of ring oscillator level, vertical nanowire FETs outperform FinFETs and horizontal nanowire devices in terms of performance-energy trade-off [22].

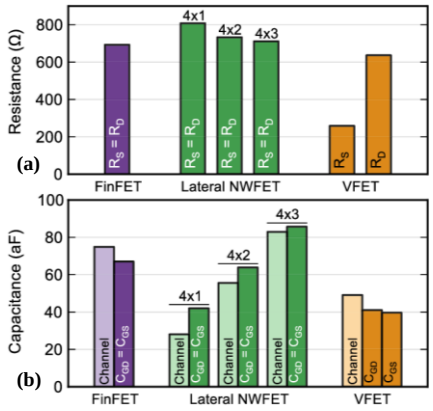

Fig. 2.9 Parasitic R and C values comparison for FinFETs, horizontal and vertical nanowire transistors for 5 nm node. From parasitic R values comparison in (a), the vertical nanowire device shows the lowest resistance compared to other device architectures. Gate-to-source C_{GS} and gate-to-drain capacitance C_{GD} in (b) exhibit lowest due to the vertical placement of insulators among gate, source and drain, reproduced from [22].

More importantly, the platform of a vertical nanowire architecture provides the convenient utilization of bandgap engineering with heterostructures, e.g. SiGeSn or III-V semiconductors in the current transport direction, this is beneficial for cutting leakage paths from the bulk substrate and reducing off-state current by using heterojunctions. What is more, it is capable of leveraging the potential of material growth with *in-situ* doping in a vertical direction. This new design freedom, not possible in the planar or horizontal configurations, makes the vertical nanowire platform more promising for CMOS scaling.

One important application for vertical nanowire transistors is Static random access memory (SRAM) in CPU cache, which is used to store bits. It also follows Moore's Law scaling with a 50% area reduction at each generation. With continuous scaling, it faces process variability, device mismatch and leakage problems. By placing two pull-up transistors on the same row in an SRAM cell, a vertical nanowire SRAM cell can provide 30% smaller layout area compared to a horizontal nanowire cell [21, 48]. Shown in Fig. 2.10 is the 3D model for 6-transistor SRAM, which shows clearly interconnect metal lines, contacts and vertical nanowire transistors. Indeed, the advantages of vertical nanowire SRAM cells lie not only in denser SRAM cells but also in providing more margin for cell improvement. For instance, the L_g and nanowire diameter relaxation by vertical architecture offers a path to optimize the variability and leakage in ultra-scaled SRAM cells, since suitably relaxed L_g and diameter can enable suppressed short-channel effects. These scaled SRAM cells also show improved read and write stability, and lowered operating voltages. In addition, to testify the role of vertical nanowire device on the circuit at 5 nm node, a 5 metal-level 32-bit multiplier design can save 19% layout area compared to that by FinFETs [49].

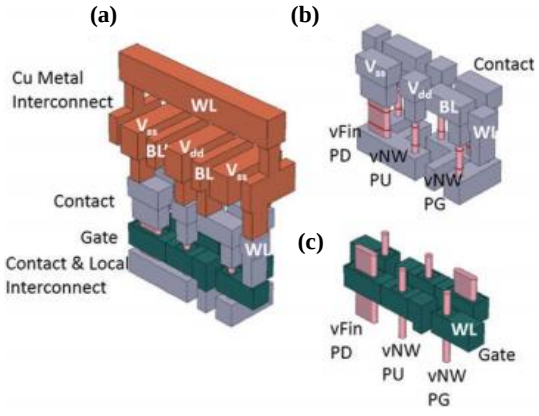

Fig. 2.10 3D model of SRAM cell (a) metal interconnect and contact layers, (b) contact and vertical devices, (c) gate contacts and vertical nanowires or fins, reproduced from [21].

In summary, as CMOS scaling continues, current FinFET technology becomes more and more difficult to provide aggressive dimensional scaling beyond 5 nm nodes. As a successor, the GAA nanowire transistor becomes a strong candidate due to the superior gate electrostatics. Vertical nanowire transistors demonstrate excellent node-to-node scalability, more layout efficiency, and less power dissipation compared to horizontal nanowire devices. Therefore, a vertical nanowire transistor should be considered as a viable path for ultimately scaled CMOS devices. However, the progress of vertical nanowire transistors still requires thorough process-design co-optimization to address the technological challenges of moving a 2D to 3D layout configuration.

2.4.2. Vertical nanowire patterning: top-down vs. bottom-up

Since the vertical nanowire platform is quite promising for ultra-scaled CMOS devices in the future nodes, herein nanowire patterning methodology is investigated. A range of approaches to pattern vertical nanowires have opened up, which in principle are categorized as the bottom-up and top-down approaches. The former includes vapor-liquid-solid (VLS), selective area epitaxial (SAE), and templated-assisted growth techniques, among which VLS mechanism is the most commonly used route with the metal droplet or particle as a catalyst during nanowire growth, e.g. Au [50-51]. However, Au atoms in Si semiconductors act as deep level traps and result in detrimental effects on electrical performance. Furthermore, Au also brings in contamination to the growth chamber and processing instruments, resulting in incompatibility with Si-based processing techniques.

As a contrast, top-down methods have demonstrated their superiority in achieving good reproducibility and precise control of the diameter and position of nanowires by employing standard CMOS processing techniques. For this purpose, the whole process comprises planar epitaxial material growth with desired stack layers, optical lithography or electron beam lithography (EBL), and reactive ion etching (RIE) or wet chemical etching. For this point, vertical nanowires can benefit from the mature planar epitaxy with complex heterostructures. In general, the top-down approach has been widely adopted in the semiconductor industry, for example, billions of fins with extremely thin width and high yield were developed at 14 nm node as shown in Fig. 2.4 (b). Within the scope of this thesis, vertical nanowires patterning by top-down paradigm is conducted and developed.

2.5. Motivation for Ge(Sn)

The first transistor in history was invented based on bulk germanium semiconductor in 1947, and Ge had been the predominant semiconductor through the 1950s, until the Si MOSFET became technologically significant. Si has a large bandgap than Ge, resulting in low leakage current in transistors, besides, perfect Si/SiO_2 combination makes Si MOSFETs the mainstream in the IC industry. In the past decade, Si MOSFETs has undergone a series of innovations to extend Moore's Law, as is discussed in section 2.2. However, recently, there is an increasing emphasis on high performance and low power targets. To this end, searching for non-silicon high mobility semiconductors is under progress. Increasing carrier mobilities can allow the improvement of on-state drive current even at a lower supply voltage, thus enhancing device performance and reduce power consumption. Although this relationship seems to be ambiguous in the quasi-ballistic regime for the ultra-scaled nodes, the high mobility materials always afford high injection velocities, and therefore, the general rules continue to apply [52-53].

2.5.1. High mobility Ge(Sn) channel materials

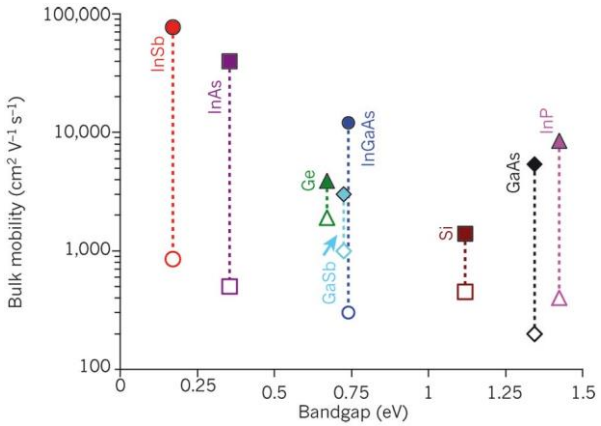

Fig. 2.11 The mobility landscape among Si, Ge and a variety of group III-V semiconductors. Filled symbols indicate electrons and open symbols indicate holes. Ge provides the highest hole mobility of any known semiconductors, while III-V semiconductor provides the highest electron mobility, reproduced from [54].

Fig. 2.11 summarizes the semiconductor landscape in terms of bulk carrier mobilities and bandgap among Si, Ge and a variety of III-V semiconductors [54]. The electron mobility of III-V materials shows great superiority with over 10000 $cm^2V^{-1}s^{-1}$ compared to Si [54] and numerous research on III-V based nMOSFETs have been conducted to demonstrate the

viability to replace Si channel in low power logic applications, however, the corresponding hole mobility in III-V is appreciably lower than the electron counterpart. This performance asymmetry by III-V nMOS and pMOS transistors makes it unpractical. What is more, the cost for III-V growth in wafer-scale is extremely high and III-V device processing is not compatible with Si-based industrial techniques.

Based on the comparison in Fig. 2.11, Ge semiconductor shows the bulk electron mobilities with 3900 $cm^2V^{-1}s^{-1}$, which is twice of hole mobility with 1900 $cm^2V^{-1}s^{-1}$. This is favorable to use the same Ge material for both n-type and p-type transistors and preferable for the performance match of Ge CMOS transistors, which is similar to the widely adopted Si CMOS logic circuit. It is noteworthy that Ge has the highest hole mobility among the known semiconductors. Significant progress on Ge based pMOSFETs has been achieved with high performance by the academia and the industry, and there is an increasing consensus that Ge can be the best option for pMOSFETs in the future nodes [55-67]. As for Ge nMOSFETs, additional challenges, e.g. reducing the density of interface traps (D_{it}), improving Ohmic contacts should be overcome to maximize the Ge-based CMOS gains. This point will be further discussed in the following chapters.

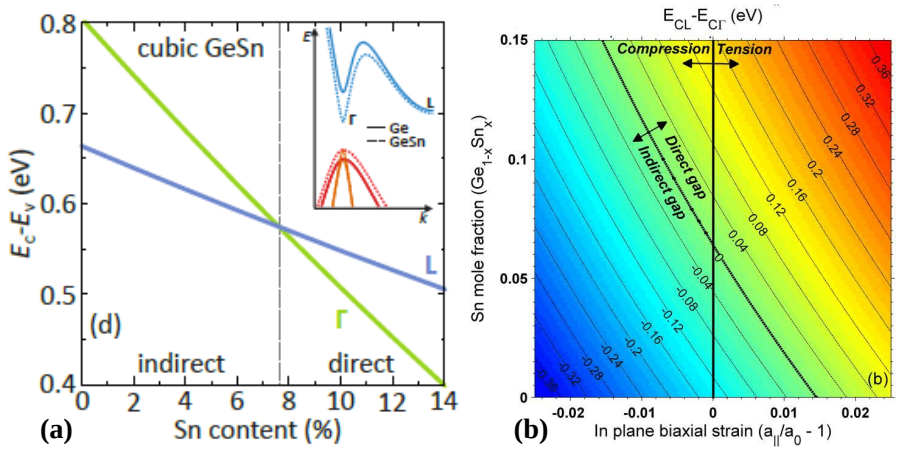

Fig. 2.12 (a) Bandgap transition with Sn composition dependence for unstrained GeSn, With the Sn composition over approximately 8%, GeSn can achieve the direct bandgap. The inset shows the exemplary band structure of Ge and $Ge_{0.89}Sn_{0.11}$. (b) The energy separation between the Γ and L conduction band as a function of Sn composition and in-plane biaxial strain. With more compressive strain in the GeSn layer, the higher Sn composition is required to achieve direct bandgap, reproduced from [72].

Additionally, the possibility of incorporating Sn element into Ge, known as GeSn alloy, has been explored for the potential electronic applications. GeSn alloy was first studied by C. Goodman in 1982 [68]. However, it takes a long time until the first GeSn-based transistor

was experimentally reported as proof of performance booster for Ge-based devices in 2011[69]. The first GeSn optically-pumped laser was achieved to show the direct bandgap transition in 2015 [70]. Whereas Ge is an indirect semiconductor with the conduction band minima at the L-point, α-Sn is a semi-metal with a direct but negative bandgap. If alloying Sn into Ge, the conduction band minima and whole bandgap shrink, leading to a tunable bandgap. If the Sn composition increases, the Γ-valley decreases much faster than L-valley. For a certain Sn composition, GeSn can achieve a transition from a fundamentally indirect bandgap to a direct bandgap. This is quite advantageous for GeSn-based photonics, e.g. lasers or detectors, and may necessitate the possible implementation of monolithic integration of GeSn-based microelectronic and photonic applications. Fig. 2.12 (a) shows the bandgap transition with Sn composition for unstrained GeSn [71]. With the Sn composition over approximately 8%, GeSn can achieve the direct bandgap, as is confirmed by the $Ge_{0.89}Sn_{0.11}$ in the inset.

α-Sn has a lattice constant of 6.493 Å, which is 14% larger than Ge (5.658 Å). As a result, GeSn layer grown on Ge will be essentially compressively strained and relaxes when exceeding a critical thickness. The strain effect has a significant influence on the band structure of GeSn, which cannot be neglected with the consideration of strain engineering in transistor design. Usually, compressive strain tends to increase the Γ-valley while decreasing L-valley, opposing the transition of the direct bandgap. As a contrast, tensile strain is beneficial for direct bandgap transformation. Fig. 2.12 (b) illustrates the energy separation between the Γ and L conduction band as a function of Sn composition and in-plane biaxial strain [72]. With more compressive strain in the GeSn layer, the higher Sn composition is required to achieve direct bandgap.

GeSn alloy is a new group IV semiconductor, which has unique electrical properties. Comprehensive studies of GeSn band structure have been conducted by first principles calculation [71-75]. It shows that the effective masses of electrons in Γ- and L-valley, light hole (LH) and heavy hole (HH) are decreased with increasing Sn composition and therefore indicates GeSn owns high carrier mobilities. This fact is also confirmed by experimental observation in GeSn-based transistors in Ref. [69, 74-79]. It should be noted that GeSn growth is conducted under a low thermal budget, leading to vacancy point defects in the epitaxial layer. These defects will act as trapping or scattering centers for electrons and holes, hampering the mobility improvement.

2.5.2. Challenges for Ge(Sn)-based FETs

Considering the economical cost for Ge-based applications and compatibility with conventional Si-based manufacturing process, it is imperative to heterogeneously integrate Ge layers on Si substrates compared to purely developing Ge wafers. Therefore, a thin epitaxial Ge layer is incorporated on low-cost Si wafers. However, to guarantee the high-quality crystalline Ge layers, growth challenges to overcome the 4% lattice mismatch between Ge and Si should be taken into account. Otherwise, the substantial numbers of dislocations in the thin Ge layer would deteriorate carrier mobility and junction leakage, which is detrimental for normal transistor operation. To accommodate the large lattice mismatch, innovative growth methods have been introduced. A thick SiGe buffer layer growth with graded composition is straightforwardly used to reduce the defect density [80-81] and it is also possible to grow a thick Ge layer directly onto Si while keeping defect density reasonably low [82]. In addition to the buffered growth of Ge, several alternative ways have been investigated. Non-coalesced aspect-ratio-trapping epitaxy was developed to grow Ge and SiGe within narrow oxide trenches to terminate threading dislocations at the trench sidewall interface [83-84]. With this technique, high-performance Ge pFinFETs were reported with good quality scaled Ge Fins [85-87]. In addition, wafer bonding [88], condensation [89-91] and liquid-phase epitaxy [92-93] techniques have been studied for Ge integration on Si.

With the well-developed Ge layer growth, GeSn epitaxial growth tends to be more realistic although significant challenges still hamper the epitaxy with high Sn composition and good layer quality. One problematic point is the low solid solubility of Sn atoms in Ge (< 1%), which limits high Sn incorporation. GeSn with high Sn content is prone to be thermodynamically metastable and Sn atoms are easy to segregate or precipitate during growth. It is noted that high thermal treatment should be avoided during device processing, e.g. forming gas annealing (FGA), post-metallization annealing (PMA). In addition, the lattice mismatch between GeSn and Ge also leads to the difficulty of material growth. Until now, chemical vapor depiction (CVD) and molecular beam epitaxy (MBE) methods under low temperatures have been explored to enable non-equilibrium growth and obtained good-quality films [94-98].

The main challenges facing Ge(Sn)-based MOSFETs arise from the small bandgap E_G, which directly reflects the increase in leakage current due to the band-to-band tunneling (BTBT). What's more, the large dielectric constant (ε_{Ge} = 16.2) tends to induce the short-channel effects compared with Si. One potential solution is to introduce heterostructures, e.g. SiGe/Ge,

GeSn/Ge, in order to suppress gate-induced drain leakage (GIDL). Besides, the incorporation of Si towards SiGeSn can lift Γ-valley with an increased bandgap, opposing the introduction of Sn. It thereby provides an additional degree of freedom in the design of bandgap engineering with heterostructures. With a large range of tunable lattice constant and thermal balance between Sn and Si, heterostructure combination, e.g. Ge/SiGeSn, GeSn/SiGeSn can also satisfy the requirement for high performance and low power logic transistors in the future sub-5 nm nodes.

Regarding MOSFET modules, high-quality interface passivation between Ge(Sn) and dielectric has to be developed due to the relatively high D_{it}. Innovative passivation methods for Ge(Sn)-based transistors should be thoroughly investigated to decrease D_{it}. Another factor facing Ge(Sn) is the strong Fermi-level pinning close to the valence band E_V, this results in a challenge for n-type Ohmic contact for nMOSFETs. Fermi-level depinning or increasing the n-type dopant concentration in Ge(Sn) is thus preferred. These two key modules will be studied in detail in chapter 3 and solutions targeting at Ge(Sn)-based vertical GAA nanowire transistors will be proposed in following chapters.

3. Fabrication process development

Contents

As discussed in Chapter 2, to further extend Moore's Law beyond sub-5 nm technology nodes, the goal of this thesis is to demonstrate Ge(Sn)-based vertical GAA nanowire MOSFETs and investigate the functionality and scaling technology of such devices. The vertical nanowire architecture proposed in this work enables p-type and n-type transistors in Chapters 4 and 5, and can also support the application of tunneling FET, memory devices, etc. Therefore, a complete process flow for vertical nanowire devices is developed with various critical modules: nanowire patterning, digital etching, gate stack, planarization, etc. At each module, relevant background and a brief literature overview are provided and compared. The fabrication techniques conducted in this chapter form a solid base for the transistor demonstration in the rest of this thesis.

3.1. Process overview

Fig. 3.1 depicts the key process modules for Ge(Sn)-based vertical GAA nanowire transistors. The device fabrication starts with the material epitaxy. Stacked material growth with high

crystalline quality and desired doping profile with the *in-situ* method is performed with reduced-pressure CVD epitaxial growth on 200 mm Si(100) wafers. Typical material design for homostructures and heterostructures is shown in Fig. 3.2. Fig. 3.2 (a-b) show the pMOSFET design with Ge p^+-p^--p^+ and GeSn/Ge i-p^--p^+ doping profiles, while (c-d) are schematically Ge n^+-n^--n^+ and Ge/GeSn/Ge n^+-n^--n^+ stacks for nMOSFET. The detailed design guidelines based on Ge(Sn) will be discussed in the following Chapters 4 and 5, and further improvement on the material growth will also be pointed out in terms of the feedback from electrical results.

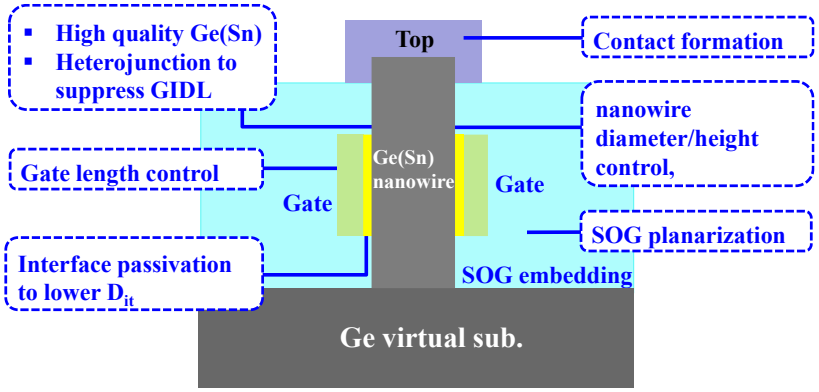

Fig. 3.1 The key process modules for Ge(Sn)-based vertical GAA nanowire transistors: high-quality material epitaxy, nanowire patterning, gate stack formation, spin-on-glass (SOG) planarization, and contacts.

After material growth, the next step will be vertical nanowire formation. It is challenging and critical to tightly control the nanowire diameter and aspect ratio. Here an optimized Chlorine (Cl_2)-based recipe using inductively coupled plasma reactive ion etching (ICP-RIE) is developed to form nanowires, followed by a digital etching process to further shrink the nanowire size and eliminate the dry etching induced damages. According to Ref. [22], vertical nanowire transistors with sub-10 nm diameter are required for ultra-scaled logic applications. Therefore, it is imperative to develop robust methods for nanowire patterning to reduce size variability and improve nanowire yielding.

Gate stack is another key module for Ge(Sn)-based MOSFETs. Interface passivation to lower D_{it} is indispensable to improve the carrier mobility, *SS*, reliability, etc. The post-oxidation method is developed in this work and is characterized by *C-V* measurement in session 3.3. The advantage of vertical gate length definition lies in independence on lithography, but the SOG planarization technology. Finally, ohmic contact for the source/drain region is significant, especially the top contact in the ultra-scaled nanowires, because top contact only

covers a small nanowire tip, which results in a bottleneck to improve the total resistance for vertical nanowire transistors.

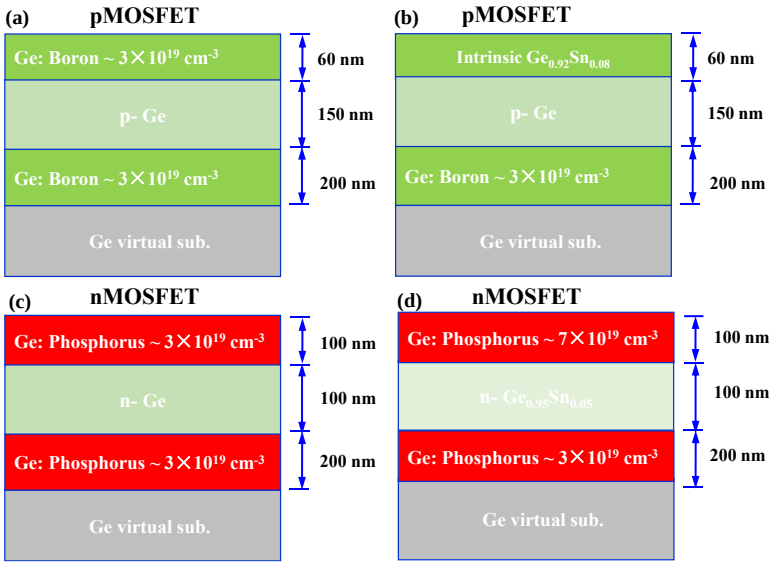

Fig. 3.2 Typical material design of homostructures and heterostructures for the pMOSFETs design with Ge p^+-p^--p^+ and GeSn/Ge i-p^--p^+ doping profiles (a-b), and nMOSFETs with Ge n^+-n^--n^+ and Ge/GeSn/Ge n^+-n^--n^+ profiles (c-d).

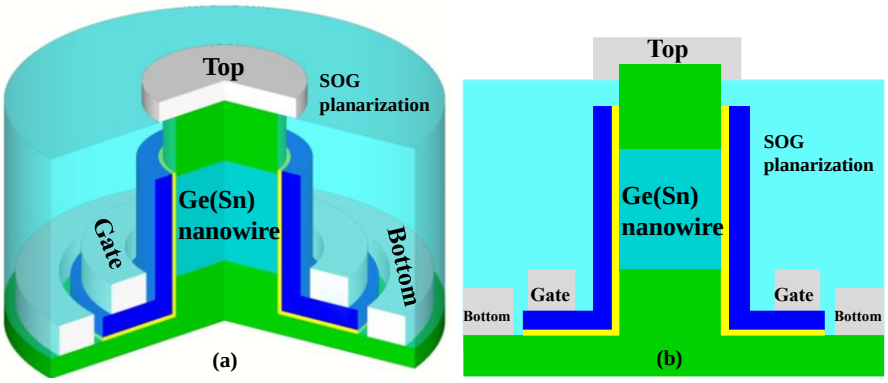

Fig. 3.3 The exemplary transistor in 3D (a) and cross-section (b) view. This design will be utilized for Ge(Sn)-based pMOSFETs and nFETs in the following chapters.

With the key process modules mentioned above, Fig. 3.3 shows the exemplary transistors in this work in 3D and cross-sectional view, respectively. Different material stacks in Fig. 3.2 for both pMOSFETs and nMOSFETs will be applied for process development, performance characterization, and further improvement in the following chapters.

3.2. Vertical nanowire formation

As is mentioned in session 2.4.2, nanowire patterning has two paradigms: top-down and bottom-up, the former will be highlighted in this work and adopted to pattern Ge(Sn) vertical nanowires. This universal method has been widely used in the applications of CMOS, sensors, photonics, energy harvesting, etc. It starts with pattern definition, here using EBL, followed by pattern transfer and then digital etching to shrink the nanowire diameter to the nanoscale level.

3.2.1. Pattern definition-EBL

EBL refers to a maskless lithography method of scanning a focused electron beam to pattern nanoscale features on a wafer surface, which is different from photolithography with light. The resolution of EBL can achieve precision level down to 1 nm due to the shorter wavelength associated with 10-100 keV electron energy. Therefore, it is always used for ultra-scaled patterns.

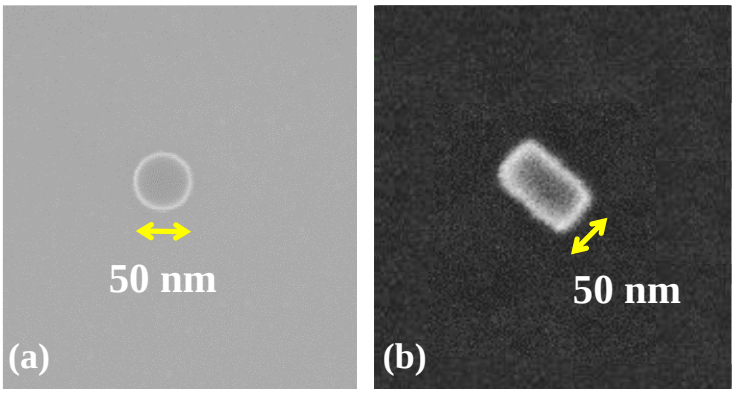

Fig. 3.4 (a) Top view of a circular HSQ pattern with HMDS and a 50 nm diameter. (b) a rectangle HSQ pattern without HMDS. After development, the HSQ pillar cannot stand up and collapses.

In this work, a strain-relaxed Ge layer on a Si wafer works as the virtual substrate for nanowire formation. Negative resist Hydrogen SylsesQuioxane (HSQ) diluted with Methyl—IsoButyl-Ketone (MIBK) is spin-coated serving as EBL resist and RIE mask. Various electron beam doses taking into account proximity effects are set for nanowires with diameters ranging from 50 nm to 100 nm. To avoid the HSQ pattern collapse after development, hexamethyldisilazane (HMDS) is applied for adhesion promotion. On a water-free substrate surface, the mehyl groups of HMDS will be exposed to form a hydrophobic

monolayer that will aid in resist adhesion. Top views of HSQ pattern with and without HMDS are shown in Fig. 3.4. The left figure in (a) shows a circular shape with a diameter of 50 nm with HMDS, while (b) exhibits the collapsed HSQ pattern without HMDS. This phenomenon should be taken into account if the diameter is further scaled below 50 nm.

3.2.2. Pattern transfer-RIE

In the top-down vertical nanowire patterning, RIE step is a critical process module, aiming at Ge(Sn) nanowires with smooth sidewalls, high aspect ratio, as well as vertical profiles. Group-IV vertical nanowires for transistor applications have been fabricated with Cl_2, Cl_2/BCl_3, Cl_2/HBr, SF_6/O_2 recipes [48, 99-103]. In this work, Cl- and F- based chemistries are applied to pattern Ge(Sn) nanowires with diameters down to sub-50 nm. To achieve vertical nanowires without obvious undercutting and micro-trenching effects, dry etching recipes are optimized with carefully calibrating gas flow, chamber pressure, RF power, and temperature.

To illustrate the role of various etching parameters on the nanowire profile, systematic studies are conducted on the vertical Ge nanowires (Diameter = 100 nm) in Fig. 3.5 in terms of etching rate, verticality, undercutting, and micro-trenching effects by Cl_2/Ar chemistry. All the samples still have HSQ hard mask on top of nanowires. Fig. 3.5 (a-b) compare the nanowire profiles with RF power of 25 W and 50 W. For these two cases, a clear undercutting effect is seen probably due to enhanced isotropic etching by reactive radicals underneath HSQ hard mask. While increasing RF power to over 80 W, the situation of undercutting becomes better and the nanowire profile has more verticality (not shown here), because the radicals get more kinetic energy, diminishing isotropic etching. Furthermore, micro-trenching is related to the bombardment of the reflected ions from the sidewall. The nanowire in Fig. 3.5 (b) exhibits an improved micro-trenching effect compared to Fig. 3.5 (a), because there is more directional vertical ion bombardment with higher energy, thus reducing ions bouncing off the sidewall. This is consistent with the result in Ref. [99]. In short, the whole etching process is contributed by two parts: Cl_2-based reactive etching and Ar-based physical sputtering. When RF power is low, Cl_2-based reactive etching dominates, resulting in more isotropic etching and smooth sidewall surface, while increasing RF power leads to more directional Ar sputtering and minimized undercutting/micro-trenching effects.

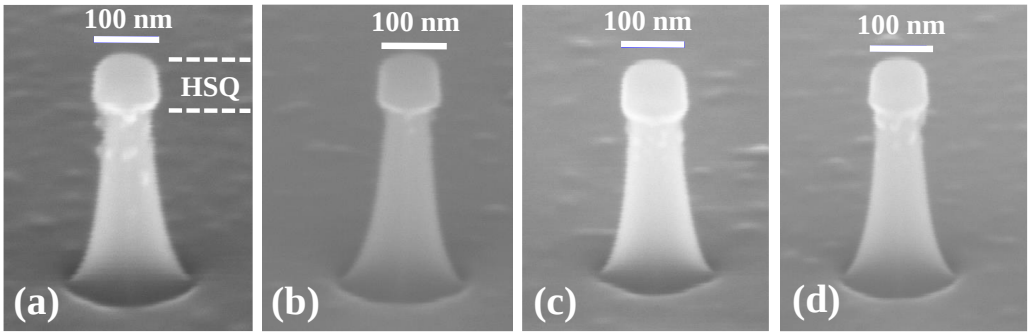

Fig. 3.5 Tilted SEM images of vertical Ge nanowires etched under various ICP-RIE conditions with the parameters listed in Table I. (HSQ resist on top) (a)-(d).

When chamber pressure is reduced from 0.005 mBar (Fig. 3.5 (a)) to 0.003 mBar (Fig. 3.5 (c)), the nanowire profile shows less obvious undercutting. At the atmosphere of 0.003 mBar, the mean free path of particles is relatively long and the reactive particles are less, which are beneficial for enhanced anisotropy. An improved micro-trenching is also obtained. This could be explained by that the collision probability among particles at low pressure is reduced, leading to decreased ion specular reflection. In addition, the surface roughness in Fig. 3.5 (b) and (c) seems slightly reduced compared to that in Fig. 3.5 (a).

Fig. 3.5 (d) is obtained at the RIE temperature of 0 ℃ (other conditions unchanged). From the etching profile comparison between (a) and (d), the undercutting and micro-trenching effects exhibit no big difference. However, the substrate temperature has a remarkable impact on surface roughness. When the temperature is decreased from 20 ℃ to 0 ℃, the sample surface roughness is improved. The residual $GeCl_x$ at low temperature is relatively easy to be pumped away, resulting in a much cleaner surface.

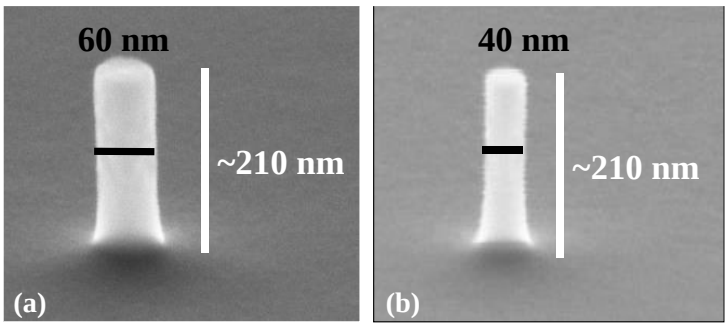

Fig. 3.6 Tilted SEM images of well-defined vertical Ge nanowires with optimized etching conditions. The nanowires show excellent verticality and smooth sidewalls.

After investigating the role of each etching parameter on nanowire formation, the optimized nanowires with high anisotropy and minimized undercutting/micro-trenching effects are

obtained (Cl_2/Ar: 4/24 sccm, RF/ICP power: 80/500W, chamber pressure: 0.004 mBar, 0 ℃). The etching rate is ~ 6 nm/s and the selectivity to the HSQ hard mask is approximately 10:1. The well-defined Ge nanowires with D = 60 and 40 nm are shown in Fig. 3.6 with excellent verticality and smooth sidewalls, which form the basis for the following vertical Ge nanowire transistor fabrication. With the same optimized parameters applied to the SF_6/Ar recipe, it leads to a higher etching rate as well as the formation of the grassing effect at the surface. This recipe still needs more investigation if F-based chemistry will be used.

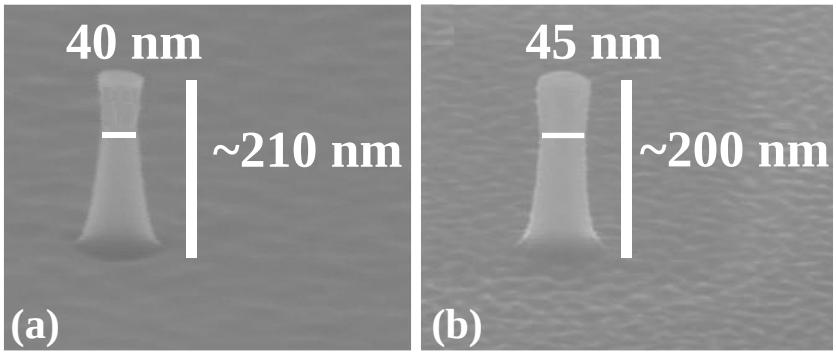

Fig. 3.7 Tilted SEM images of vertical nanowires with GeSn/Ge (a) and Ge/GeSn/Ge (b). The planar surface for both nanowires is not perfectly smooth due to the introduction of the Sn element in GeSn during Cl_2/Ar etching. High-temperature etching, e.g. 200 ℃ can solve this problem.

As is stated in Fig. 3.2, bandgap engineering with Ge(Sn)-based heterostructures are highlighted for vertical nanowire devices in this work, which implies the well-developed recipe should own minimal etching selectivity between Si, Ge, and Sn elements during nanowire etching. Fig. 3.7 depicts SEM images for GeSn/Ge and Ge/GeSn/Ge heterostructure nanowires corresponding to Fig. 3.2 (b) and (d), respectively. They show the vertical nanowire profile and smooth sidewalls. However, the planar surfaces for both nanowires are not perfectly smooth due to the introduction of the Sn element in GeSn during Cl_2/Ar etching [104-105]. It's reported that $SnCl_x$ by-products are non-volatile at low temperatures, therefore, these by-products are redeposited as hard masks at 0 ℃, which roughens the planar surface. High-temperature etching, e.g. 200 ℃ can alleviate this problem.

3.2.3. Digital etching

The RIE recipe associated with various chemistries unavoidably induces plasma-based damages due to high energy ion bombardment. As a consequence, the nanowire sidewall surface could be deteriorated by long time exposure to plasma. The current conduction

mechanism in MOSFETs lies in surface modulation where the carriers transportation is in proximity (only a few nanometers) to the surfaces. Plasma-induced point defects and interface nonstoichiometric states play a critical role in device performance and reliability degradation, such as deteriorated carrier mobility, *SS*, I_{ON} [106-108]. Therefore, it is of paramount significance to improve the nanowire sidewall for an excellent oxide/channel interface.

To cope with these issues, the Si nanowires and fins are treated with high-temperature H_2 annealing (~ 850 ℃), providing a great method to yield atomically smooth sidewall surfaces [109-112]. Besides, high-temperature thermal oxidation followed by stripping Si oxide in acids can also contribute to smooth vertical nanowires [113-114]. However, high thermal budget processing does not apply to Ge(Sn), especially GeSn with high Sn compositions. At too high temperatures, Sn tends to diffuse, segregate, and probably forms β-Sn precipitations, resulting in damage to material integrity.

To eliminate the sidewall surface damage and further shrink the nanowire diameters to improve the gate electrostatic control, digital etching techniques consisting of nanowire oxidation and oxide removal are developed. In order to keep a low thermal budget for Ge(Sn), the oxidation step is performed by exposing the nanowires in O_2 plasma atmosphere at room temperature and then rinse the nanowires in diluted hydrochloric acid (HCl) or hydrofluoric acid (HF) for 1 min to remove the oxide. By repeating these two steps, the scaled Ge(Sn) nanowires can be obtained in a controlled way.

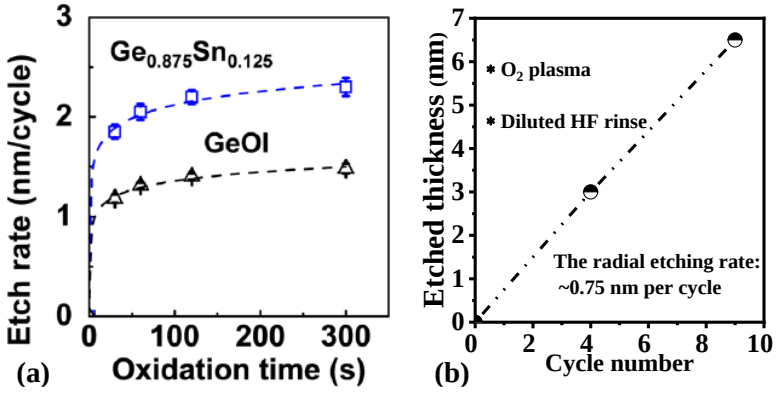

Fig. 3.8 (a) Etching rate as a function of O_2 plasma exposure time for Ge and $Ge_{0.875}Sn_{0.125}$. It increases rapidly for the first 120s and then saturates fast to certain rates for Ge and GeSn, reproduced from [115]. (b) Radial etching thickness of Ge nanowire in terms of cycle number. From the curve, it is observed a linear fit with the extracted radial etching rate of ~0.75 nm per cycle.

The oxidation of Ge(Sn) is logarithmic with the oxidation time and then gets a fast saturation [115]. Fig. 3.8 (a) shows the etching rate as a function of O_2 plasma exposure time for Ge and

$Ge_{0.875}Sn_{0.125}$ [115]. It increases rapidly for the first 120s and then saturates to certain rates for Ge and GeSn. The rule does not follow the Deal-Grove model rigorously for thermal oxidation, which includes two processes: one is the chemical reaction at the interface and the other is the diffusion of oxygen through the generated oxide film. The process of O_2 plasma oxidation is similar to the thermal oxidation except for the atomic diffusion of O atoms through the oxide layer. A complementary model of the Deal-Grove theory was proposed to explain the O_2 plasma oxidation kinetics in Equation 3.1. The logarithmic growth limit depicts faster saturation of the diffusion-limited process compared with the parabolic limit from the Deal-Grove theory.

$$T = \frac{\mathrm{A}}{2} ln(\frac{2B(t+\tau)}{A^2} + 1) \tag{3.1}$$

Where T is oxide thickness, A and B the parameters related to the effective diffusion coefficients, t the oxidation time, τ the oxidation time for native oxide formation.

Since the oxidation is self-limiting, the etched thickness in the digital etching process is not determined by the oxidation time, but by the etching cycle numbers. In this work, the RF power of O_2 plasma is fixed at 300W, the gas flow is 200 sccm, and the pressure is 0.4 mBar. After 120s oxidation, the nanowires are rinsed in diluted HF or HCl. The radial etching thickness of Ge nanowire is shown in terms of cycle number in Fig. 3.8 (b). From the curve, a linear fit with the extracted radial etching rate of ~0.75 nm per cycle is observed.

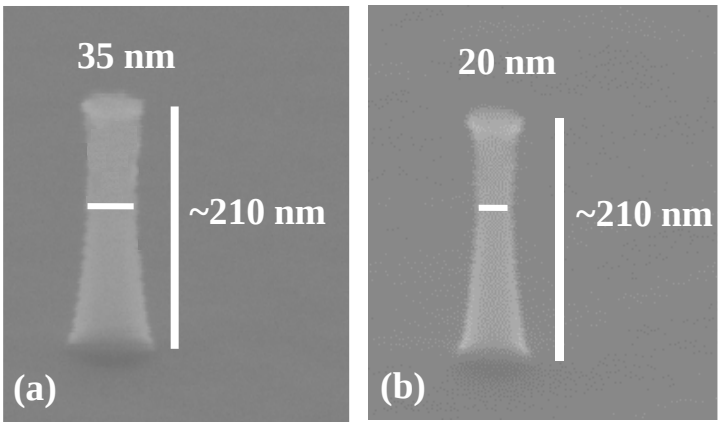

Fig. 3.9 (a) Tilted SEM image of a vertical Ge nanowire with a 35 nm diameter exhibiting a perfect anisotropy, (b) The same nanowire with a 20 nm diameter and an aspect ratio of ~10.5 after 10 cycles' digital etching.

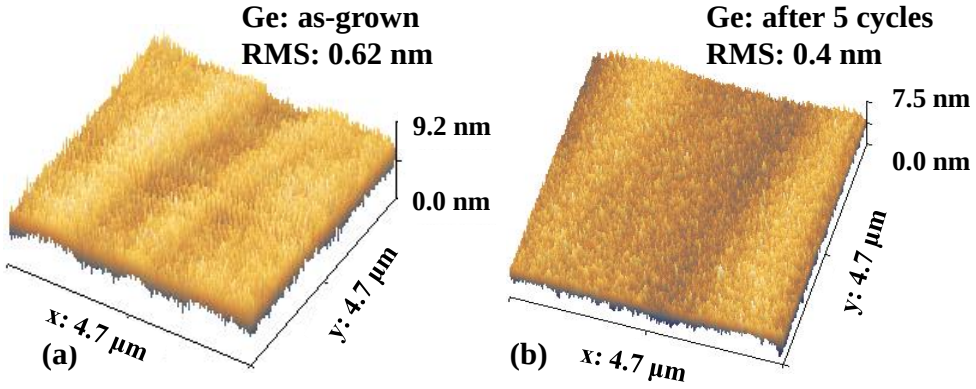

Fig. 3.10 AFM images of as-grown Ge planar sample (a) and Ge sample after 5 cycles digital etching (b). The RMS surface roughness is 0.62, 0.4 nm for both samples. Digital etching developed in this work provides a positive way to improve the surface roughness.

Fig. 3.9 (a) displays the vertical Ge nanowire with a 35 nm diameter defined by the well-developed dry etching. After 10 cycles' digital etching, the dimeter is shrunk from 35 nm to 20 nm as shown in (b). It is seen that nanowires after digital etching keep the good verticality. The 20-nm diameter nanowires are applied for transistor fabrication, which will be further discussed in Chapter 4. It is also proved that cyclic digital etching is beneficial for surface morphology [115]. An atomic force microscope (AFM) is applied to characterize the surface roughness of Ge planar samples and Ge samples after digital etching. Fig. 3.10 shows AFM images of the as-grown Ge sample and after 5 cycles digital etching, which shows root-mean-square (RMS) surface roughness of 0.62 and 0.4 nm, respectively. Digital etching developed in this work provides a positive way to improve the surface roughness.

This methodology is especially preferred for GeSn, which requires a low thermal budget. Furthermore, the GeSn oxidation rate is faster compared to Ge. This enhancement arises from weaker Ge-Sn bonds than Ge-Ge bonds since the dissociation energies for the Ge-Ge, Ge-Sn, and Sn-Sn bonds are 264.4 ±6.8, 230.1 ±23, and 187.1 ±0.3 kJ/mol, respectively [116]. As expected, it leads to a higher oxidation rate if Sn content in GeSn is increased. Besides, it is noted that the oxidation rate of Ge nanowires is also higher than the Ge bulk sample, which could be explained by the dependence on surface orientations. For vertical nanowires with a larger surface-area-to-volume ratio, there are more dangling bonds compared to Ge planar surface, leading to an increased oxidation rate.

The noteworthy concern for ultra-scaled vertical nanowires is the processing variability. Fig. 3.11 shows the vertical nanowires with 14 and 15 nm diameters. With the variation in dry etching and digital etching processes, the small nanowire profile cannot keep uniform. As a consequence, a robust and reproducible etching method should be developed. Atomic layer

etching (ALE) is an emerging technique in semiconductor manufacturing, which consists of alternating etching between self-limiting chemical modification and etching step to remove the chemically-modified areas, allowing the removal of individual atomic layers. It is a high-precision process to keep atomic-scale fidelity of the size and composition for transistors beyond 5 nm nodes. Additionally, to avoid small nanowire collapse in the possible wet etching step, it is reported that alcohol-based wet etching can provide a smaller surface tension compared to aqueous etching, which contributes to the yield of ultra-scaled nanowires [117].

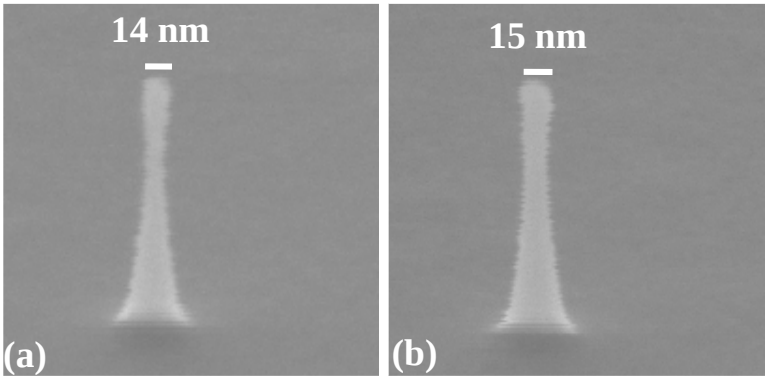

Fig. 3.11 Tilted SEM images of vertical nanowires with 14 and 15 nm diameters, showing the processing variability. The profiles are not the same. A robust and reproducible etching method should be developed to minimize profile variability.

Another issue related to ultra-scaled vertical nanowires is the nanowire sidewall characterization. Due to the lack of proper metrology techniques, nanowire line edge roughness until now has been only detected by eyes from SEM images and is beyond SEM detection capability (Cross-sectional TEM is difficult to perform on vertical ultra-scaled nanowires). Moreover, sidewall stoichiometry for small nanowires is different from that of the bulk sample, possible dopant segregation and Sn loss at the sidewall surface should be taken into consideration during the electrical analysis of transistors.

3.3. Gate stack

The MOS structure with SiO_2/Si combination has been continuously adopted to pursue high performance and low power Si CMOS applications in the past half century. This is because SiO_2/Si is perfectly matched with excellent thermal stability and a low D_{it} at the interface. However, this is extremely challenging for Ge-based MOSFETs, considering that the native oxide of Ge, GeO_2 is thermally unstable and readily decomposes into GeO_x sub-oxides. It

results in a high density of dangling bonds at the interface. Therefore, the intrinsically high carrier mobility of Ge becomes overshadowed due to the trap charge scattering at the interface. Besides, it can also affect the leakage current, *SS*, I_{ON}/I_{OFF} ratio, etc. It is imperative to look for the appropriate dielectrics on Ge with the performance comparable to the state-of-the-art SiO_2/Si.

Oxides with high permittivity (high-κ) were introduced to replace SiO_2 from 45 nm nodes since they can provide a larger physical thickness while maintaining a low *EOT*. *EOT* uses the equivalent SiO_2 thickness as the metric to gauge the strength of the gate capacitance, which is defined as

$$EOT = t_{high-\kappa}\left(\frac{\kappa_{SiO_2}}{\kappa_{high-\kappa}}\right) \tag{3.2}$$

Where $t_{high\text{-}\kappa}$ is the thickness of high-κ oxide and κ is the relative dielectric constant for SiO_2 and high-κ oxide.

For instance, a high-κ oxide such as HfO_2 with $\kappa \approx 18$, can obtain the same gate capacitance as SiO_2 with $\kappa \approx 3.9$ while the physical thickness is 4.6 times larger than SiO_2. With this high-κ oxide, the physical thickness with 2.3 nm is enough to suppress the gate leakage and keep the same gate efficiency as 0.5 nm SiO_2, which would induce an appreciable gate leakage.

The shift to high-κ oxide has diminished the significance of the SiO_2/Si interface and enabled continuous transistor scalability. Numerous high-κ dielectric on Ge research has been conducted in terms of minimal D_{it}, appropriate band stoichiometry with Ge, sufficiently high breakdown voltage, good thermodynamic, and kinetic stability, etc. The appropriate band alignment between high-κ dielectric with Ge requires the conduction and valence band offsets should be at least 1 eV to reduce the injection of carriers into the dielectric, which is another source of gate leakage. Fig. 3.12 (a) shows the calculated band alignment of high-κ oxides on Ge [118]. From the point of view of band alignment, these common oxides are suitable for MOSFET applications. Other than this, the choice of high-κ dielectrics is also determined by the κ values and their bandgap. Fig. 3.12 (b) summarizes the κ values and experimental bandgap for common dielectrics [119]. The κ values tend to vary inversely with the bandgap. There are some oxides with extremely large κ value, e.g. ferroelectric $BaTiO_3$, but they own a very small bandgap. Indeed, too large κ oxide is undesirable for MOSFETs due to strong parasitic capacitance coupling between gate and source/drain contacts. In summary, from these candidates comparison, the most promising high-κ dielectrics are Al_2O_3, HfO_2, and ZrO_2. They are greatly considered because of their relatively higher dielectric constant, appropriate band alignment with Ge, sufficiently high breakdown voltage, and reasonable

thermal stability. Atomic layer deposition (ALD) is the usual way to produce highly conformal and pinhole-free insulting high-κ films with precise thickness control on the sub-nm scale. And great progress with these high-κ dielectrics in MOSFETs has been made.

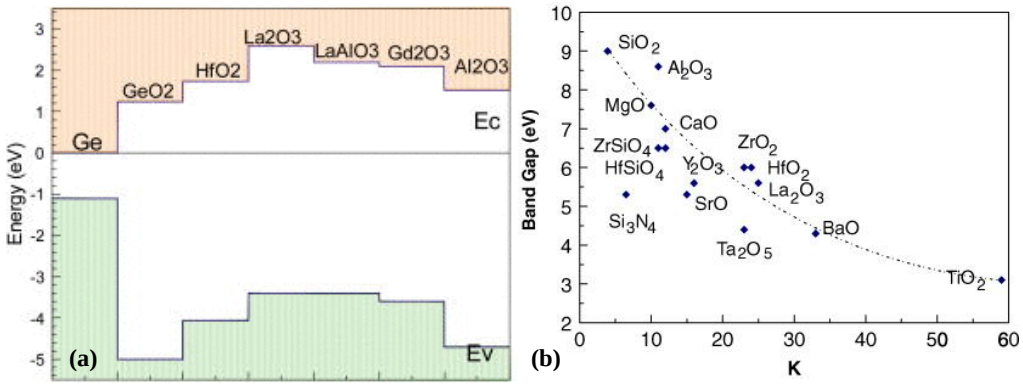

Fig. 3.12 (a) The calculated band alignment of high-κ oxides on Ge. The conduction and valence band offsets between high-κ oxides and Ge should be at least 1 eV to reduce the injection of carriers into the dielectric, reproduced from [118]. (b) The static dielectric constant and experimental bandgap for common dielectrics, reproduced from [119].

High-κ dielectrics have a higher density of defects compared to SiO_2. The defects at the interface can lead to a high D_{it} and act as scattering centers, while the defects within the dielectric would also affect the mobility by remote optical phonon scattering [120], remote Coulomb scattering [121] and surface roughness scattering [122-123]. What is more, during thermal treatment in the transistor fabrication, Ge and high-κ dielectrics could interdiffuse, namely, Ge-Hf bonds, resulting from GeO_x/HfO_2 interdiffusion, produce defects in the Ge bandgap and therefore a large D_{it} [124-125].

To address this issue, an interfacial layer (IL) is particularly formed between high-κ dielectrics and Ge channel prior to high-κ oxide deposition. The IL has a lower dielectric constant and a lower density of defects, which can passivate the Ge surface. However, the incorporation of IL tends to increase the total *EOT* by the high-κ dielectric and IL in series, which is computed as follow:

$$EOT_{tot} = t_{high-\kappa}\left(\frac{\kappa_{SiO_2}}{\kappa_{high-\kappa}}\right) + t_{IL}\left(\frac{\kappa_{SiO_2}}{\kappa_{IL}}\right) \tag{3.3}$$

Where κ_{IL} and t_{IL} are the dielectric constant and the physical thickness of IL, respectively.

The addition of IL hampers the further *EOT* scaling. It sparked many research interests to look for promising passivation methods in terms of the balance between the *EOT* scalability

and high-performance gate stack. To date, the most promising approaches have been explored to generate ILs for passivation, e.g. surface nitration [126-129], sulfur passivation [130-131], thin epi-Si [57, 59-60, 63-66, 85-87, 132-140], high quality GeO_2 growth [61, 141-150]. Here GeO_2 growth is highlighted in detail.

3.3.1. GeO_2 IL passivation

Since Si native oxide SiO_2 has been used to sufficiently passivate Si surface, it also sparked numerous research interests on Ge native oxide as the passivation layer, usually written as GeO_x. Because it is primarily composed of a mixture of GeO and GeO_2. GeO_x is water-soluble and GeO_2 is thermal-dynamically unstable and transforms to GeO at approximately 420 ℃. It is reported that the presence of lower oxidation states of GeO_x and Ge-metal bonds due to the interdiffusion between GeO_x and high-κ dielectrics can lead to extrinsic states in the Ge bandgap and thereby degraded carrier mobility [124-125, 151-154]. Nevertheless, good quality GeO_2 has been considered as a promising IL due to the potential for both Ge p- and nMOSFETs [61, 136, 141-144]. Peak electron mobility of ~ 1100 cm^2/Vs was obtained for Ge nMOSFETs with thick GeO_2 (~20 nm), which was generated by high-pressure oxidation followed by a low-temperature oxygen annealing [145]. Other oxidation methods, e.g. ozone oxidation [146], thermal oxidation [147], have been also explored to achieve high electron mobility at a low D_{it} of 10^{11} eV^{-1} cm^{-2}. However, these high mobility results are at the cost of large *EOT*. Apparent mobility degradation was observed with decreasing GeO_2 thickness.

The desire to form an ultrathin GeO_2 passivation layer between a high-κ dielectric and underlying Ge channel is required to simultaneously achieve low D_{it} and *EOT*. The quality of GeO_2 IL is strongly dependent on the oxidizing species, such as atomic oxygen, ozone, or molecular oxygen [148, 154]. And the principle is to generate higher oxygen states of GeO_2 with respect to other sub-oxide species. One promising development to balance carrier mobility and *EOT* scalability is the post-oxidation method [141-143, 149-150]. With high-κ dielectric stacks e.g. $HfO_2/Al_2O_3/GeO_2$ IL, Ge p- and n-MOSFETs can maintain high hole and electron mobilities at a low D_{it} level. What is unique about this scheme is an ultrathin Al_2O_3 layer is deposited, followed by O_2 plasma or ozone exposure to grow GeO_2 IL underneath the Al_2O_3, here the Al_2O_3 layer serves as an oxygen diffusion barrier to control the thickness and quality of GeO_2. Later on, high-κ dielectrics are deposited to reduce gate leakage and keep a low *EOT*. It is reported that to suppress the tendency of Ge to diffuse into a high-κ dielectric layer, Al_2O_3 is resistant to the Ge up-diffusion, which is beneficial for the high-performance gate stack [125]. Moreover, ZrO_2 or HfO_2/GeO_2 stack is found to intermix during ALD as well as the partial reduction of Ge^{4+}, while Al_2O_3/GeO_2 behaves very well

[154]. This method provides a viable way to passivate Ge surface and decent electrical performance has been obtained for Ge planar [155-159], Fin [136, 160], and horizontal nanowire MOSFETs [144, 161-162]. Based on these studies, the post-oxidation scheme is directly applied to vertical Ge GAA nanowire MOSFETs in this work.

Nevertheless, although the great progress in boosting both electron and hole mobilities has been demonstrated by excellent GeO_2/Ge interface, the purpose of simultaneously achieving high mobility and superior reliability is still a challenge [138-140]. Thorough investigations should be conducted before the GeO_2 IL passivation method will be applied to high-volume manufacturing.

Compared to the surface passivation upon Ge MOSFETs, there is not so much research on GeSn MOSFETs primarily due to the difficulty of material growth and complex processes. In short, two passivation methods are summarized for GeSn FETs as: thin Si IL [69, 77, 163-168] and GeO_2 IL with post-oxidation passivation [169-171]. The former is formed by *in-situ* Si_2H_6 passivation at a low temperature (~ 370 ℃). With this scheme, $Ge_{0.92}Sn_{0.08}$ quantum well pMOSFETs achieve record-high hole mobility of 845 cm^2/Vs at the capacitance equivalent thickness of 2.2 nm [77]. GeSn pFinFETs with sub-10 nm Fins show decent subthreshold properties and transconductance [165-167]. In addition, GeSn horizontal nanowire pMOSFETs with post-oxidation passivation have been obtained with high I_{ON}, also indicating good quality gate stack [169-171].

3.3.2. Gate stack with post-oxidation passivation

According to what is mentioned above, high-performance gate stack engineering is of the great essence for Ge(Sn)-based low power logic applications. Here high-κ dielectric/metal gate stack with post-oxidation passivation is applied and investigated for vertical Ge(Sn) GAA nanowire MOSFETs.

After digital etching, the samples are rinsed in diluted HF/HCl (1:1) and immediately loaded into an ALD chamber for 1 nm Al_2O_3 deposition at a heater temperature of 250 ℃ using Trimethylaluminium (TMA) as the precursor and water vapor as co-reactant, followed by a post-oxidation process with thermal or plasma process. A thin GeO_x IL is thus generated underneath Al_2O_3. Next, 8 nm Al_2O_3 is deposited. Moreover, for the purpose of EOT scaling, HfO_2 with tetrakis (ethylmethylamino) hafnium (TEMAH) precursor is also used. Subsequently, 40 nm TiN gate metal is sputtered conformally wrapping around the nanowire as shown in Fig. 3.14 (a). It shows a tilted SEM image of a vertical nanowire with a TiN/Al_2O_3/GeO_x gate stack. Note that the TiN sputtering in this work leads to conformal coverage with a sidewall thickness roughly half of that on the planar surface. This is

confirmed by a cross-sectional TEM image of the high-κ/metal gate stack on the nanowire sidewall, as clearly depicted in Fig. 3.14 (b). The thickness of TiN metal in the sidewall is ~ 20 nm, approximately half of 40 nm in the planar surface. To obtain a completely conformal coverage of gate metal, atomic vapor deposition (AVD) is one option, based on pulsed precursor injection CVD. Since horizontal GAA nanowire transistors will be potential mainstream beyond sub-5 nm nodes, the conformal metal deposition is particularly indispensable for GAA applications.

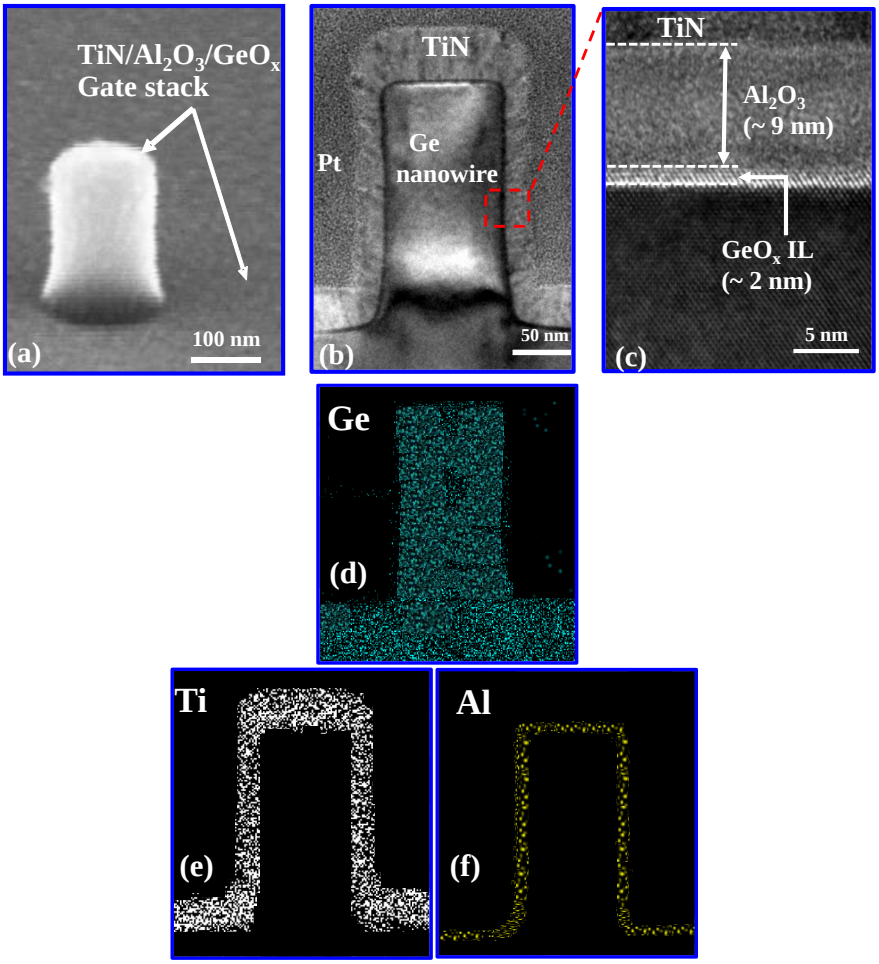

Fig. 3.14 (a) Tilted SEM image of a Ge nanowire after Al_2O_3 deposition and TiN sputtering. Ge nanowire was wrapped around by the gate stack. (b) Cross-sectional TEM image of a vertical Ge nanowire with a TiN/Al_2O_3/GeO_x gate stack. (c) HR-TEM image of the gate stack, depicting the excellent quality of the gate stack and good crystallinity of Ge channel. (d-f) EDX mapping of Ge (cyan), Ti (white), and Al (yellow) atoms with sharp contours for TiN/Al_2O_3/GeO_x gate stack on a Ge nanowire. Focused Ion Beam (FIB) was used for TEM lamella preparation.

Fig. 3.14 (c) shows a high-resolution TEM (HR-TEM) image of gate stack with 9 nm Al_2O_3 and ~2 nm GeO_x IL generated by post-oxidation passivation. It also demonstrates the excellent quality of the gate stack and excellent crystallinity of the Ge channel. Energy-dispersive X-ray Spectroscopy (EDX) mapping of elemental Ge, Ti, and Al for $TiN/Al_2O_3/GeO_x$ gate stack on Ge nanowires shows sharp contours, proving clear interfaces and good conformity of gate stack (Fig. 3.14 (d)-(f)).

The MOS structure is a fundamental module for the well-performing MOSFETs and also a versatile method to characterize the quality of high-κ dielectric and high-κ dielectric/semiconductor interface. However, it is difficult to measure the capacitance-voltage (C-V) curves for ultra-scaled vertical nanowire MOS capacitors (MOScap) considering the negligible capacitance. What is more, the processing of fabricating the vertical nanowire MOScap would be complicated. Therefore, MOScaps on planar Ge samples are chosen to characterize the gate stack.

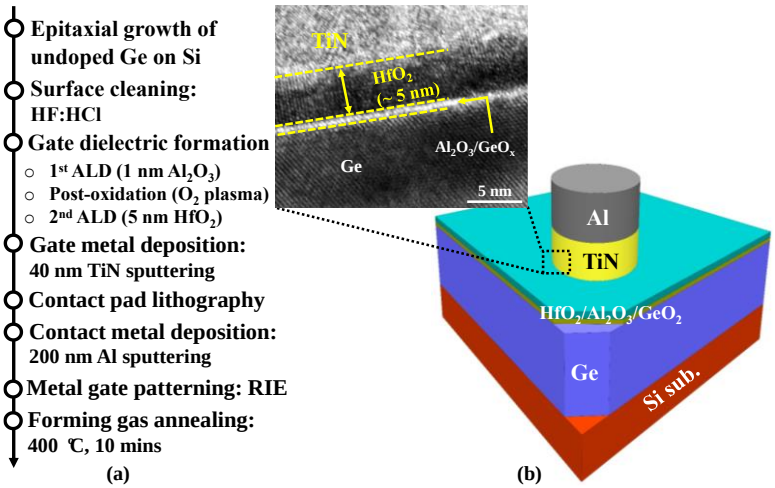

Fig. 3.15 (a) The key process flow for MOScap fabrication. (b) 3D MOScap schematic and the cross-sectional TEM image of a $TiN/HfO_2/Al_2O_3/GeO_x$ gate stack on Ge, demonstrating high Ge crystalline quality and smooth interfaces.

The fabrication process of a MOScap is straightforward. It starts with Ge surface cleaning (HF: HCl rinse), followed by the ALD deposition. The post-oxidation passivation described above is applied. For the high-κ dielectric, HfO_2 and Al_2O_3 are used for the following applications in the vertical nanowire MOSFETs. A 40 nm TiN gate metal is deposited via reactive sputtering. The Al contact pad is patterned by lithography and lift-off processes, which also acts as a hard mask in the gate metal patterning by dry etching. Finally, the fabrication ends with forming gas annealing (FGA) with 400 ℃, for 10 mins. The key process

flow is summarized in Fig. 3.15 (a). Fig. 3.15 (b) depicts a 3D MOScap schematic and the cross-sectional TEM image of a TiN/HfO_2/Al_2O_3/GeO_x/gate stack on Ge, demonstrating high Ge crystalline quality and smooth interfaces.

It is noted that unlike the traditional top-to-back MOScap, the MOScaps in this work are arranged as top-to-top. This means, the probe with high voltage is applied to a capacitor with a small area, while the other capacitor has an area which is several orders of magnitude larger. Then the C-V characteristics are dominated by the small capacitor as both capacitors are connected in series. Therefore, the equivalent C-V curves for small MOScaps are obtained.

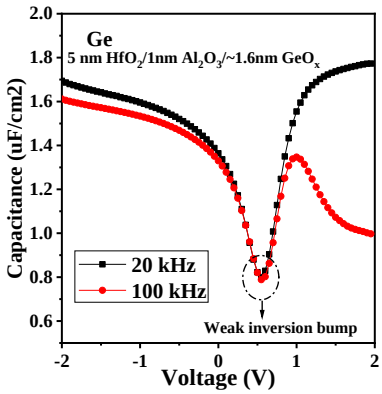

Fig. 3.16 Typical C-V characteristics of Ge MOScap with TiN/HfO_2/Al_2O_3/GeO_x gate stack with 20 kHz and 100 kHz. The MOScap exhibits good switching characteristics, without a flat-band voltage shift over these two frequency ranges. In the depletion region, the minimum capacitance approaches ~0.78 μF/cm^2, indicative of the weak inversion bump.

Fig. 3.16 displays the typical C-V characteristics of Ge MOScap with TiN/HfO_2/Al_2O_3/GeO_x gate stack at the frequencies of 20 kHz and 100 kHz. The curves exhibit well-behaved switching characteristics, without a flat-band voltage shift over these two frequency ranges. At 100 kHz, the C-V curve cannot follow the frequency response and drops down in the inversion region. Slight frequency dispersion in the accumulation region can be observed probably due to the series resistance. What is more, in the depletion region, the minimum capacitance approaches ~0.78 μF/cm^2, indicative of the weak inversion bump. This is typical for small bandgap materials, such as Ge, GeSn, or InGaAs. Because minority carrier response is more obvious due to thermal carrier generation with a small bandgap E_G. This also leads to the difficulty to quantitatively estimate D_{it}. Usually, the conductance method is a common and reliable way to extract D_{it} from C-V and conductance-voltage (G-V) measurement [172-173]. However, it cannot be directly applicable to low-bandgap materials. On one hand, D_{it} for these materials is generally larger, it leads to the series capacitance contributed by the interface traps and also stretch-out effect by filling interface traps from accumulation to

inversion region especially in low frequencies. On the other hand, a frequency-dependent D_{it}-induced bump in the depletion region could also be confused with weak inversion bump, thus overestimating the true value of D_{it}. A novel D_{it} extraction method should be developed to characterize a high-κ dielectric/channel interface on low-bandgap semiconductors.

In addition, Ge MOScap with HfO_2/GeO_x is also fabricated. From the C-V curves, it shows a large hysteresis window. There are several factors which should be taken into account: i) mobile ionic charges, e.g. Na^+ inside the dielectric during ALD is quite related for the hysteresis; ii) the intermixing of Ge-Hf leads to the dangling bonds at the border or within the HfO_2/GeO_x, forming the so-called slow traps. The time constant of charging in slow traps is too large to follow the alternating-current (AC) frequency response, but they can follow the slow direct-current (DC) sweeping speed. This can also lead to hysteresis in the I-V measurement for transistors.

3.4. Planarization

In the vertical nanowire structures, planarization is an indispensable module as an insulator layer. Spin-on-glass (SOG) coating and etch-back bring convenience to precisely control the insulator layer planarization to obtain a flat topology, which is highlighted in this work. The insulator layer is used to isolate the 3D-level contact electrodes (gate, source, and drain) as shown in Fig. 3.3, the requirements for an insulator layer are low dielectric constant to minimize parasitic capacitances, perfect planarity property, and good thermal and mechanical stability. HSQ resist is one promising SOG, whose properties are similar to silicon oxide after curing at high temperature or electron beam bombardment. It is reported that with a highly diluted HF (1:1000), the etch-back control of HSQ film can achieve a nanoscale etching rate of ~ 1 nm/s, which is beneficial for surface planarization [175]. For this purpose, the etch-back process can be also achieved by dry etching with carefully optimizing etching parameters.

During HSQ planarization for vertical nanowires, a major consideration is the wave effect in proximity to the nanowires. It causes the insulator thickness variation, as schematically shown in Fig. 3.17(a). The corresponding SEM image in Fig. 3.17 (b) depicts two nanowires with gate stack covered by HSQ and the wave effect with the upslope close to the nanowire is especially illustrated. To circumvent the wave effect issue, one viable way is to embed the vertical nanowires in the HSQ layer by making use of its flowable property in Fig. 3.17 (c). Considering the maximum thickness of HSQ film that the spin-coating can achieve, multiple

coating is required to fully submerge the nanowires. It is noted that during each coating step, curing at high temperature is a key for multiple coating to avoid dissolution of the resist film coated before. The curing process for HSQ is to chemically stabilize the layer at a moderate temperature (300-600 ℃) in the N_2 atmosphere (to inhibit cracking in the layer). It will transform the cube-like structure to a network-like structure by the scission of Si-H bonds and the formation of siloxane bonds [176]. Typically, ~10 nm reduction in HSQ film after curing is observed by the ellipsometry compared to as-coated film in this work.

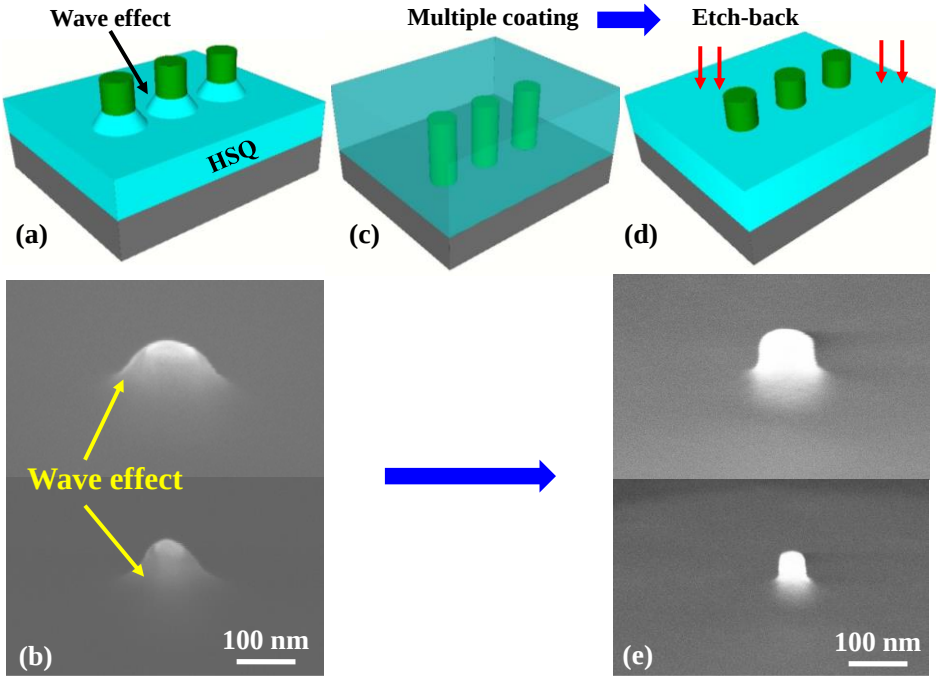

Fig. 3.17 (a) 3D schematic of a vertical nanowire after HSQ spinning. The wave effect in proximity to the nanowires is clearly observed. (b) SEM image of two nanowires with gate stack covered by HSQ, also showing the wave effect with the upslope close to the nanowire. (c) Multiple coating to embed the vertical nanowires in the HSQ film by making use of its flowable property. (d) Etch-back to planarize the HSQ film to the desired position. An optimized dry etching recipe based on CHF_3 with a tight control etching rate of 10 nm/min is well-developed. (e) SEM image of two nanowires with the optimized etch-back method, showing a quite uniform film thickness.

Afterwards, the HSQ layer needs etch-back to position the desired height as shown in Fig. 3.17 (d). Hence, an optimized dry etching recipe based on CHF_3 is well-developed with a tight control of the etching rate of 10 nm/min for the planarization. Shown in Fig. 3.17 (e) is the optimized HSQ planarization with quite uniform film thickness.

In summary, the well-developed planarization method with HSQ spinning and etch-back can be directly applied in the vertical nanowire device fabrication. In this work, there are two planarization steps in total: top gate stack recess and spacer isolation, as schematically illustrated in Fig. 3.18. The first planarization starts with a vertical nanowire with a gate stack in Fig. 3.18 (a), which also corresponds to Figs. 3.14 (a-b). T_{M} is the TiN metal thickness on top of nanowires and T_{top} is the distance between the junction edge and the dielectric on top of nanowires. Afterwards, the planarization step follows the multiple spin-coating, curing, and CHF_3 etch-back steps (Fig. 3.17). The schematic in Fig. 3.18 (b) corresponds to the SEM images in Fig. 3.17 (e). T_{O} means the overlap distance above the junction edge. To get the desired etch-back thickness, T is thus determined by $T_M + T_{top} - T_O$. This step has to be aligned accurately through multiple ellipsometer measurements and SEM monitoring.

Subsequently, the top gate stack recess is conducted, exposing the top nanowire for the top contact formation shown in Fig. 3.18 (c). An optimized SF_6/Cl_2/Ar-based recipe is developed to isotropically remove the TiN metal, especially on the nanowire sidewalls. It is worth noting that the high-κ dielectrics (HfO_2 or Al_2O_3 in this work) has a large etching selectivity to this recipe compared to TiN, therefore, they are expected to cover and preserve the top nanowires. What is more, these etchants also have a bit impact on HSQ etching, which is not reflected in Fig. 3.18 (c). Fig. 3.19 (a) displays a typical SEM image of a nanowire with top gate stack recess at this process stage (HSQ is removed for a good view).

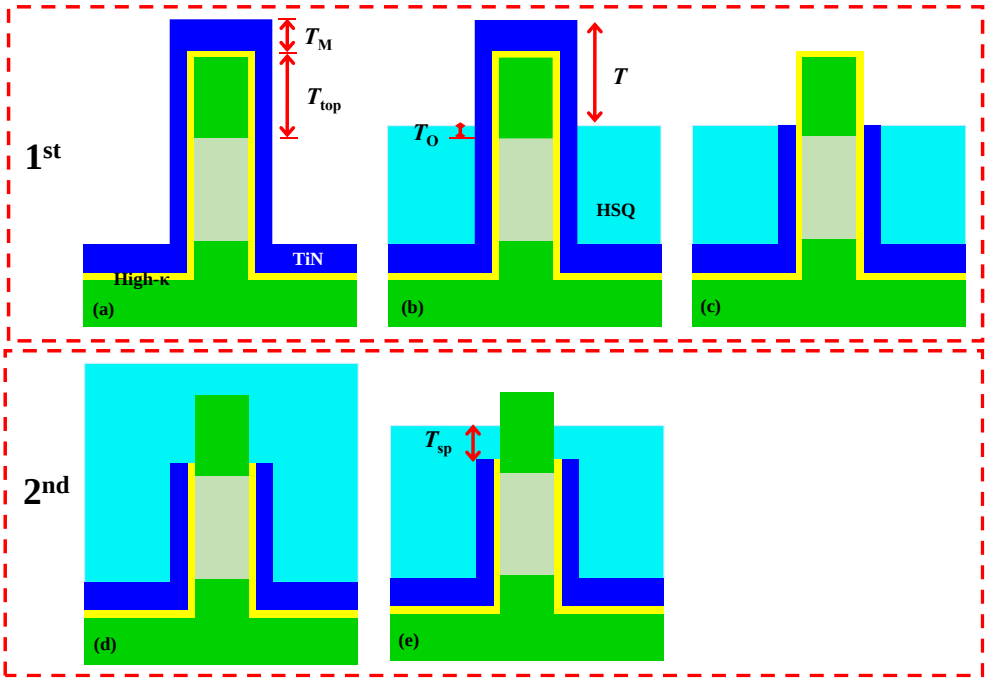

Fig. 3.18 (a) Cross-sectional schematic of a vertical nanowire with gate stack. T_M is the TiN metal thickness on top of nanowires and T_{top} is the distance between the junction edge and the dielectric on top of nanowires. (b) The 1st planarization with multiple coating and etch-back processes. To get the desired etch-back thickness T, this step has to be aligned accurately through multiple ellipsometer measurements and SEM monitoring. (c) Top gate stack recess, exposing the nanowire for the top contact formation. An optimized SF_6/Cl_2/Ar-based recipe is developed to isotropically remove the TiN metal, especially on the nanowire sidewalls. (d) The 2nd planarization starting with multiple spin-coating. (e) Etch-back step with careful monitoring to keep the spacer thickness appropriate for the top contact and isolation purposes.

In order to insulate the gate stack from the top contact which is formed later, the second planarization process is conducted as shown in Figs. 3.18 (d-e). It also goes through multiple spin-coating, curing, and etch-back steps. T_{sp} is the spacer isolation distance, the principle of T_{sp} determination is to leave the top nanowire exposure as large as possible for small top contact resistance while keeping T_{sp} appropriate to minimize the coupling between the top contact and gate stack. By carefully monitoring the etch-back process, 10-15 nm T_{sp} is typically targeted. It is noted that considering the process variation, the planarization step has to be calibrated each time, otherwise, it would result in potential performance differences. Fig. 3.19 (b) describes the SEM image of 2nd HSQ planarization for gate-to-top contact spacer isolation. The top 30 nm nanowire is exposed for the top contact formation.

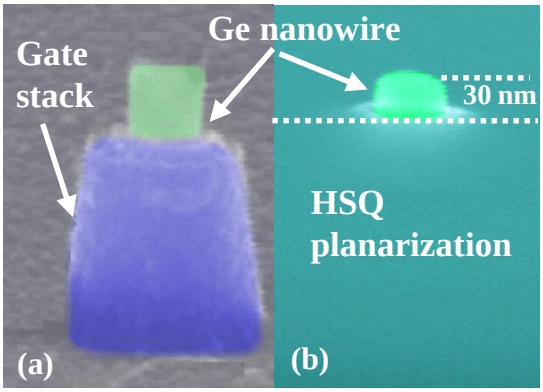

Fig. 3.19 (a) A typical false-color SEM image of a nanowire with top gate stack recess, TiN on the nanowire sidewall is isotropically removed. HSQ is removed for a good view. (b) The SEM image of 2nd HSQ planarization for gate-to-top contact spacer isolation. The top 30 nm nanowire is exposed for the top contact formation.

3.5. Contact

Due to the aggressive downscaling of transistor features as is discussed in Chapter 2, device performance improvement, e.g. I_{ON}, switching speed, is also restrained by the increasing

parasitic series resistance. It is projected that at 5 nm technology node, the parasitic series resistance contributes to ~56% in the resistance components, namely, extension resistance, contact resistance, and source/drain resistance [21]. Among these, the degraded contact resistance is one of the roadblocks that should be fully addressed. For an ideal metal-semiconductor contact in a transistor, it should own a negligible contact resistance and possess Ohmic *I-V* characteristics. To achieve this purpose, lowering the specific contact resistivity ρ_c is particularly critical, which is directly related to Schottky barrier height Φ_B at the metal-semiconductor interface and active doping concentration N_D in the semiconductor as below:

$$\rho_c \propto e^{\left[\frac{4\pi\sqrt{\varepsilon_s m^*}}{h}\left(\frac{\Phi_B}{\sqrt{N_D}}\right)\right]} \tag{3.4}$$

Where ε_s and m^* are the dielectric constant and effective electron mass of the semiconductor, respectively. h is the Planck's constant.

From Equation 3.4, it is straightforward to imply that lowering Φ_B and increasing N_D are both beneficial to minimize ρ_c. Generally, at the nodes beyond 5 nm, ρ_c lower than 10^{-9} **Ω**-cm^2 is required to alleviate the impact of contact resistance [177]. The common method for Si/Ge-contact is called silicidation or germanidation, which goes through a proper annealing process to form silicide or germanide. Numerous researches have been conducted to explore suitable metals, e.g. Co, Ti, Ni, Pt, at various formation conditions [178].

Regarding n- and p-type Ge-metal contacts in CMOS devices, the ideal combination would be perfectly aligning germanide Φ_B with either E_C or E_V for electrons and holes, respectively. That is, proper metals with low work functions form a small Φ_B, favorable for electron transportation in nFETs, while metals with large work functions would be beneficial for holes in pFETs. However, the fact that there is a significant D_{it} at Ge-metal interface leads to the Fermi level pinning effect, which is, the band alignment across the interface is essentially independent of chosen metals even with a large work function range. Then Φ_B for electrons can be written as [118]:

$$\Phi_B = S(\Phi_M - \Phi_S) + (\Phi_S - \chi_S) \tag{3.5}$$

Where Φ_M and Φ_S are work functions of metal and reference energy of Ge interface states, respectively. χ_S is the electron affinity of Ge. These energies are referred to as the vacuum level. S is a dimensionless Schottky pinning parameter, which is:

$$S = \frac{1}{1 + \frac{e^2 D_{it} \lambda}{\varepsilon_{Ge}}} \tag{3.6}$$

Where e is the electron charge, D_{it} is the density of interface states, λ is the decay length into Ge, ε_{Ge} is the permittivity of Ge.

S reflects the strength of Fermi level pinning. As D_{it} is 0, then S = 1, meaning no pinning effect, while if D_{it} is large enough, S = 0, describing the Bardeen limit of strong pinning where Equation 3.5 applies. Typically, S is in the range of 0.02-0.05 for Ge [179-180].

In Fig, 3.20 (a), it shows the band alignment between various metals and Si/Ge [181]. For Ge, all of the metals with different work functions have Fermi levels strongly pinned close to the valence band edge, which corresponds to very small S. Hence p-type contacts are relatively easy to fabricate with a small Φ_B for holes. Recently, low contact resistivity ρ_c at sub-10^{-9} Ω-cm^2 has been demonstrated with high doping concentration for Ti-Ge p-type contacts [182-185]. With the additional Sn into Ge, Φ_B for holes is further lowered and ρ_c as low as 4.1 ×10^{-10} Ω-cm^2 can be obtained [185]. High-performance Ge pMOSFETs have been already achieved in planar, Fin, and horizontal GAA nanowire structures [55-57, 64-66]. However, the most challenging issue is the n-type counterpart due to the strong Fermi level pinning and thereby a large Φ_B for electrons.

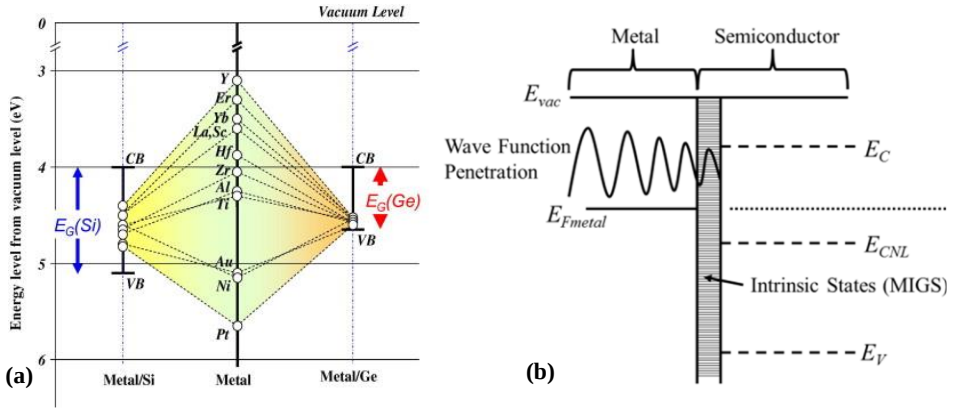

Fig. 3.20 (a) Band alignment between various metals and Si/Ge. Almost all of the metals with different work functions have the Fermi level pinned near the valence band edge, which is beneficial for holes, reproduced from [181]. (b) Physical description to interpret Fermi level pinning due to the penetration of metal wave function into the Ge side, resulting in the metal-induced gap states.

From a point view of physical description for Fermi level pinning, the band alignment depends on how strong the charge transfer is via the wave function tailing across the interface

shown in Fig. 3.20 (b). Electrons from the metal charge the intrinsic interface states within the bandgap, which form metal-induced gap states (MIGS) [118]. These states tend to be donor-like traps in the lower half of the bandgap and acceptor-like traps in the upper half of the bandgap. The transition position between these traps is termed as charge neutrality level (CNL).

Considering a good n-type contact, Fermi level depinning methods have been under exploration. It is reported by the insertion of a thin layer of GeO_2 [186], TiO_x [187], Ge_3N_4 [188], sulfur passivation [189], the electron wave function is weakened in the thin layer and decouple Fermi level pinning from charge transfer. Besides, a concern for n-type Ge contact is the low activation of dopants in Ge and the solid solubility of common n-type dopants e.g. P, As, in Ge is only at a level of $\leq 10^{20}$ cm^{-3}. For instance, the active P concentration in Ge by equilibrium methods is limited to 5×10^{19} cm^{-3} [190]. Since heavy doping can promote electron tunneling through the Schottky barrier, one promising approach to increase n-type active doping concentration is ultra-fast high-temperature activation, e.g. laser annealing [191-192] or flash lamp annealing [193]. By nanosecond-pulsed laser annealing, the electron concentration of $\sim 3\times10^{20}$ cm^{-3} was achieved, and ρ_c as low as 1.5×10^{-8} Ω-cm^2 was reached by nickel germanide contact [192]. Nevertheless, the challenge related to these non-equilibrium methods remains to be how to keep the supersaturated and metastable source/drain region robust enough to undergo the following thermal processing steps.

3.5.1. N-type contact with circular TLM structure

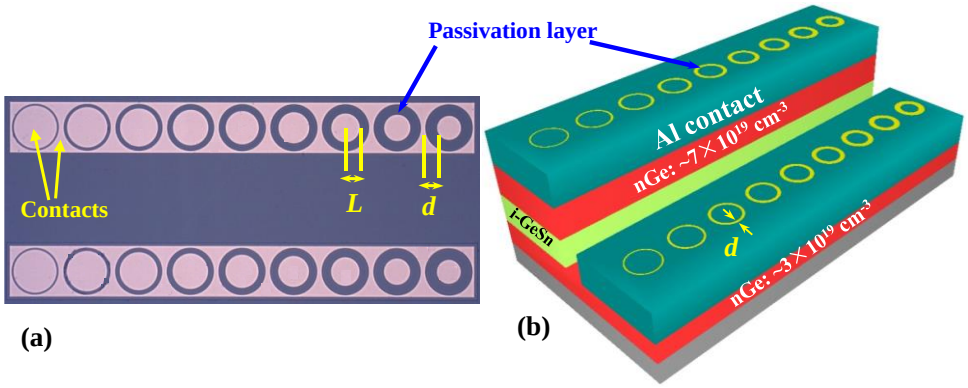

Fig. 3.21 (a) Microscopic image of CTLM test structures (top view), consisting of a circular inner contact with radius *L*, a ring-shaped gap with width *d*, and outer contact. The gap width *d* varies from 4 to 36 μm. (b) 3D schematic of CTLM structures on the top and bottom Ge layers. The active Phosphorus doping is $\sim 7\times10^{19}$ cm^{-3} and $\sim 3\times10^{19}$ cm^{-3} in the top and bottom Ge layers, respectively.

Ohmic contact characterization for n-type Ge based on the material stack in Fig. 3.2 (c-d) is conducted here. Generally, the transmission Line Measurement (TLM) with two terminal contacts is applied. Through the linear relationship between the total resistance and the contact space, typical parameters, e.g. specific contact resistivity, sheet resistance can be extracted and compared. However, the current between two contacts tends to spread due to the current crowding effect [194]. Based on this issue, circular TLM (CTLM) is proposed, consisting of a circular inner contact with radius *L*, a ring-shaped gap with width *d*, and outer contact. Fig. 3.21 (a) displays a microscopic image of CTLM test structures. The gap width *d* varies from a few microns to tens of microns.

n-Ge/i-$Ge_{0.95}Sn_{0.05}$/n-Ge material stack shown in Fig. 3.2 (d) is prepared for vertical nanowire nMOSFETs, here it is also used to characterize the Ohmic contact on the n-type top and bottom Ge layers. The material stack was grown by reduced-pressure CVD on 200 mm Si wafers with a 2.5 µm thick Ge buffer layer. It is noted that through electrochemical capacitance-voltage (ECV) measurement, the active *in-situ* Phosphorus doping is ~ 7×10^{19} cm^{-3} and ~ 3×10^{19} cm^{-3} in the top and bottom Ge layers, respectively. The doping concentration in the top Ge layer is higher due to the low-temperature growth considering the GeSn layer in the middle. The details of GeSn/Ge layer growth is not specified here and can be found in Ref. [82, 94-95, 195-196]. The next step is to etch the top and bottom Ge mesas by optical lithography and RIE. Afterwards, 15 nm Al_2O_3 and 100 nm SiO_2 are deposited in ALD and PECVD to passivate the mesas, respectively. CTLM window opening is performed by lithography and CHF_3 dry etching. Subsequently, 15 nm Ni and 200 nm Al are sputtered. FGA at 400 ℃ for 30s is done to form nickel germanide (NiGe). Fig. 3.21 (b) is a 3D schematic of CTLM structures on the top and bottom Ge layers in this work.

The CTLM is characterized by I-V measurement by simply applying the voltage across two contact metals. To acquire more accurate measurement, here four probes are applied for the measurement, two are for the I-V curves, and other two are used to sense the voltages to calibrate the external resistance in the probes. Therefore, total resistance R_{tot} as a function of gap spacing is obtained. In theory, R_{tot} across two contacts is calculated as [197]:

$$R_{tot} = \frac{R_{sh}}{2\pi}\left[\frac{L_T}{L}\frac{I_0\left(\frac{L}{L_T}\right)}{I_1\left(\frac{L}{L_T}\right)} + \frac{L_T}{L+d}\frac{K_0\left(\frac{L}{L_T}\right)}{K_1\left(\frac{L}{L_T}\right)} + \ln\left(1+\frac{d}{L}\right)\right] \tag{3.7}$$

Where *I* and *K* denote the modified Bessel functions of the first order. R_{sh} is the sheet resistance of the underlying Ge layer. L_T is the transfer length, which is the average distance

that the current flows underneath the contact. $L_T = \sqrt{\rho_c / R_{sh}}$. For $L \geq 4L_T$, the Bessel function ratios I_0/I_1 and K_0/K_1 tend to unity and R_{tot} is transformed to:

$$R_{tot} = \frac{R_{sh}}{2\pi}\left[\frac{L_T}{L} + \frac{L_T}{L+d} + \ln\left(1+\frac{d}{L}\right)\right] \tag{3.8}$$

For CTLM structure, if $L >> d$, the natural logarithm term can be simplified by Taylor expansion in Equation 3.8, then R_{tot} becomes:

$$R_{tot} = \frac{R_{sh}}{2\pi(L+d)}(d + 2L_T)C \tag{3.9}$$

Where C is considered as a correction factor.

$$C = \frac{L+d}{d} ln\left(1+\frac{d}{L}\right) \tag{3.10}$$

This means the non-linear R_{tot}~d can be simplified into a linear curve by the correction factors. This is crucial to compensate for the difference between the linear TLM and CTLM to obtain a linear fit to the experimental data.

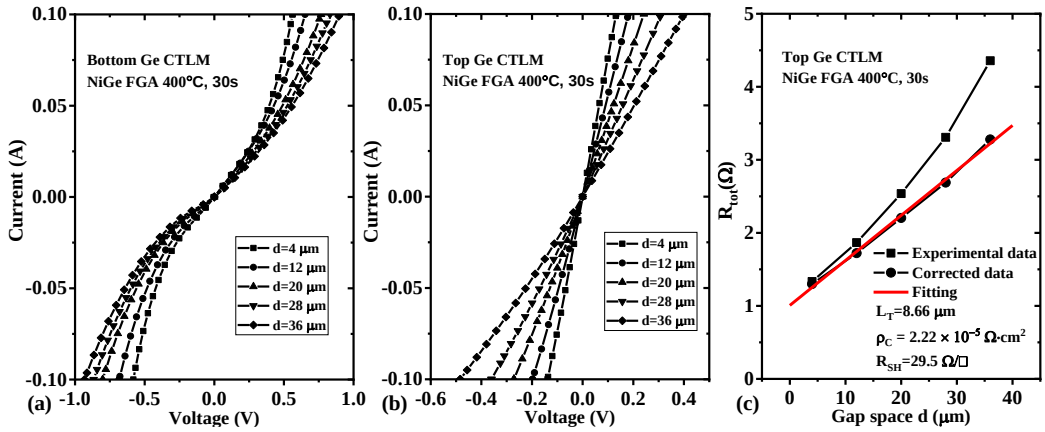

Fig. 3.22 (a) I-V curves of CTLM structures with various gap widths for the bottom Ge layer. Schottky behavior is evident. (b) I-V curves of CTLM structures for the top Ge layer with Ohmic properties. (c) R_{tot} as a function of gap space d. R_{tot} data points before correction (square) shows a non-linear trend, after correction, it becomes linear (circle). Then the transfer length, contact resistance and contact resistivity can be yielded.

Fig. 3.22 shows the CTLM characteristics for the bottom and top Ge layers after FGA. By comparing the I-V curves of CTLM structures with various gap widths in Fig. 3.22 (a), Schottky behavior is evident for the bottom n-type Ge contacts. This is because large Schottky

barrier height for electrons and a low P doping concentration of ~3×10^{19} cm^{-3} cannot afford Ohmic contact. Then the specific contact resistivity and sheet resistance are difficult to extract. As is discussed previously, the higher active P doping concentration is preferred for n-type Ohmic contacts. With a high P doping concentration of ~7×10^{19} cm^{-3} in the top Ge layer, Ohmic properties are clearly shown (Fig. 3.22 (b)). The depletion width in the Ge side is inversely proportional to the square root of the doping concentration. The width decreases as the doping concentration increases, thus, the tunneling barrier width also decreases, beneficial for the tunneling probability.

From the linear I-V curves in Fig. 3.22 (b), total resistance R_{tot} can be obtained by fitting I-V curves to allow the following extraction of specific contact resistivity and sheet resistance, etc. R_{tot} as a function of gap space d is plotted in Fig. 3.22 (c), R_{tot} data points before correction (square) shows a non-linear trend, after correction, it becomes linear as Equation 3.9 depicts. Then the transfer length and contact resistance can be yielded from the intercept with the y-axis and x-axis, respectively. Here, L_T = 8.68 μm, contact resistance R_C = 0.5 Ω. In addition, from the slope of the linear fit, R_{SH} of 29.5 Ω/□ can be calculated, provided R_{SH} is uniform in the layer underneath the metal contact and also the ring-shaped gap. Therefore, the specific contact resistivity ρ_C of 2.22×10^{-5} Ω·cm^2 is obtained. This value is a bit smaller than the NiGe contact in the same doping level [198]. Note that the high doping in the top Ge layer is performed during low-temperature growth, therefore, NiGe/Ge interface might be degraded, leading to a lowered ρ_C [199]. Robust methods to maintain high-quality Ge layer and high doping concentration should be developed to form good n-type Ohmic contacts and high-performance Ge nMOSFETs. The detailed electrical results on Ge nMOSFETs will be discussed in Chapter 5.

3.6. Conclusion

In this chapter, a detailed investigation of process modules for vertical nanowire transistors is introduced. An optimized ICP-RIE recipe based on Cl_2/Ar chemistry is developed to pattern vertical nanowires with good verticality, minimal undercutting, and micro-trenching effects. To further shrink the nanowire diameters and eliminate the dry etching-induced damages, digital etching is introduced with multiple cycles of self-limiting O_2 plasma oxidation and diluted HF or HCl rinse. Moreover, it is a high-precision etching that is capable of suppressing etching variability. With this method, a small nanowire with a 20 nm diameter and an aspect ratio of ~10.5 is obtained. Gate stack with post-oxidation passivation is discussed in detail

and is applied to Ge(Sn)-based vertical nanowire transistors. HSQ planarization includes multiple spin-coating steps of HSQ and etch-back, which shows the uniform thickness of the planarization film. In addition, how to achieve p-type and n-type Ohmic contacts for Ge(Sn) is also pointed out. These process modules in this chapter lay a solid foundation for the transistor fabrication in the rest of this thesis. Both p-type and n-type vertical nanowire MOSFETs are demonstrated and will be fully evaluated in Chapters 4 and 5.

4. GeSn/Ge vertical GAA nanowire pMOSFETs

Contents

In this chapter, the demonstration of Ge(Sn)-based GAA nanowire pMOSFETs is presented with detailed electrical analysis. It starts with the key process flow based on the process modules described in Chapter 3. This vertical nanowire platform enables vertical nanowire pMOSFETs fabrication based on undoped Ge, Ge p^+-p^--p^+, and GeSn/Ge p^+-p^--p^+ structures. With the well-functioning devices, thorough investigations of the dependence of electrical performance e.g. *SS*, $G_{m,ext}$, R_{tot}, on nanowire diameter scaling, *EOT* scaling, souce/drain asymmetry, and low temperatures are performed. It is for the first time to demonstrate vertical Ge and GeSn/Ge GAA nanowire pMOSFETs by top-down approaches. This work is intended as a proof of principles for excellent functionality and scaling technology of Ge(Sn)-based vertical nanowire transistors and also suggests strategies for further performance improvements. Parts of these results in the upcoming chapter have previously been published in Refs. [200]-[205].

4.1. Key process steps

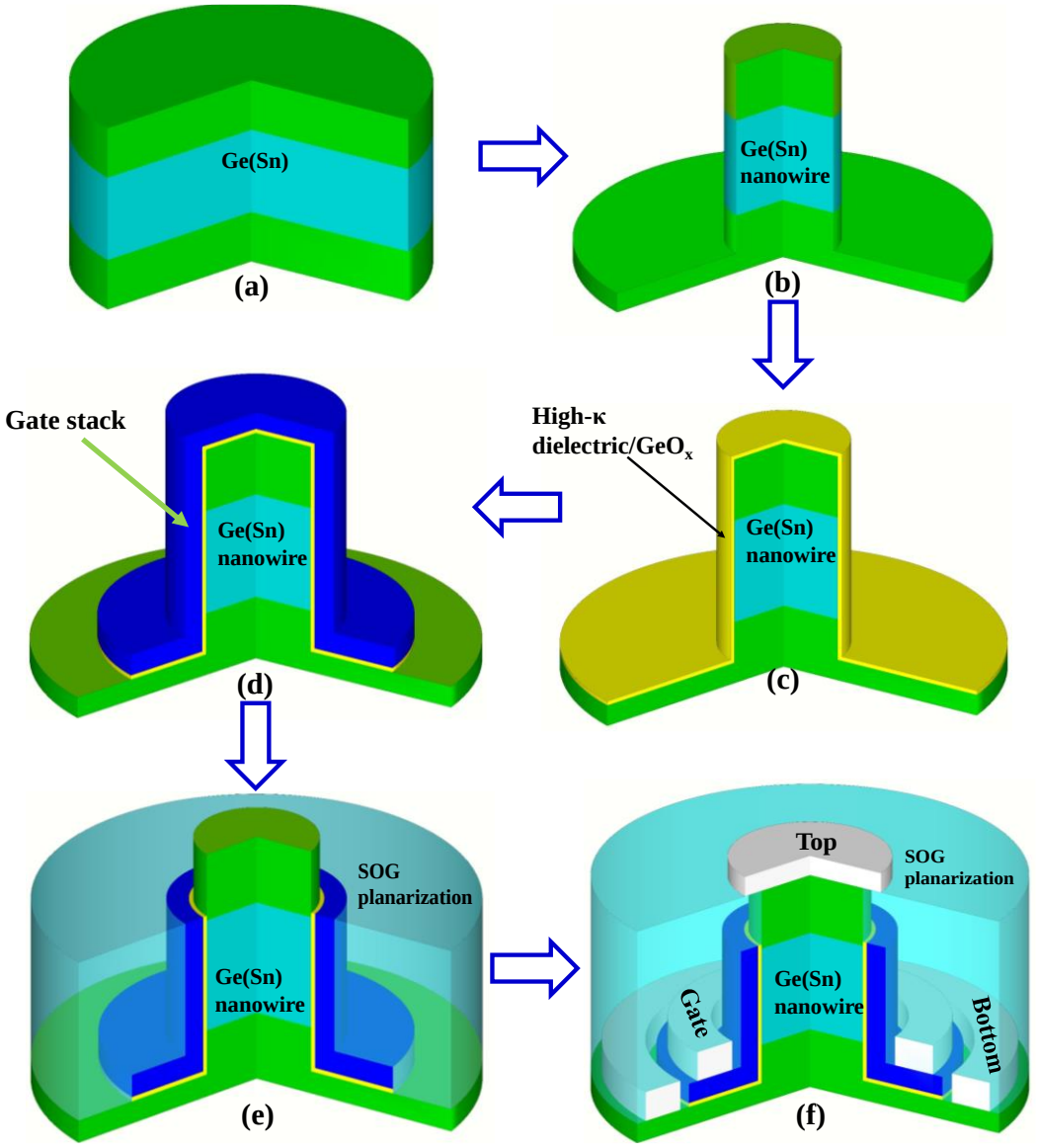

Fig. 4.1 Key process steps for vertical GAA nanowire MOSFETs. (a) Desired material epitaxy for p-type and n-type MOSFETs based on Fig. 3.2. (b) Nanowire etching and digital etching to form ultra-scaled nanowires. (c) High-κ dielectric deposition with optimized passivation. (d) Gate stack patterning followed by FGA to improve dielectric quality. (e) SOG planarization and top gate stack recess to expose the top of nanowires. (f) The device fabrication ends with contact vias opening and Ti/Al metallization.

Based on the key process modules presented in chapter 3, a complete process flow is illustrated in Fig. 4.1. The device fabrication starts with the desired material epitaxy for p-type and n-type MOSFETs, as schematically shown in Fig. 3.2. The material design guidelines will be explained in the following chapters. The epitaxy is performed on a 200 mm

Si (100) wafer with ~ 2.5 μm Ge buffer layer shown in Fig. 4.1 (a). After growth, solvent cleaning with acetone/isopropanol is done to remove the organic contaminants and particles on Ge or GeSn surface. Note that a standard Si cleaning procedure known as RCA (Radio Corporation of America) cleaning, cannot apply to Ge or GeSn materials regarding their chemical stability. E-beam lithography and optimized ICP-RIE based on Cl_2/Ar recipe are conducted to pattern vertical nanowires with various diameters. Since there are no etch-stop layers, the nanowire height is monitored by the etching time and SEM measurement. Typically, the nanowire height is in the range of 210-250 nm in this work. A digital etching technique is then performed to further thin down nanowires and improve the sidewall surface, which is shown in Fig. 4.1 (b).

In order to obtain a conformal coverage of gate dielectric and gate metal, ALD and sputtering are applied for high-κ dielectric and TiN metal deposition, respectively. Post-oxidation surface passivation is chosen for high-κ dielectrics in terms of gate leakage and EOT scalability (Fig. 4.1 (c)). Again, lithography and RIE are needed to pattern gate area (Fig. 4.1 (d)), at this step, a thick resist is spin-coated to protect the whole nanowire and be resistive to TiN etching. FGA annealing is then applied to improve the dielectric quality. As is seen, the gate metal still covers the top and sidewall of vertical nanowires. To recess the top gate stack for the top contact metallization, HSQ planarization with multiple spin-coating, curing, and etch-back steps are needed to position the physical gate length. Afterwards, the removal of TiN on the top is carried out by an SF_6/Cl_2/Ar etching, which is optimized to isotropically remove TiN on the sidewall (Fig. 4.1 (e)). Moreover, the chemical etching is selective to the high-κ dielectric, favorable for protecting the top nanowire part. In this way, the physical TiN gate length is determined by the planarization thickness of HSQ, rather than the lithography patterning commonly adopted in FinFETs or horizontal nanowire transistors. This, to a large degree, relaxes lithography scaling from gate length and contact placement scaling, a noteworthy symbol for vertical nanowire architecture. What is more, the self-aligned gate metal with small misalignment variation is highly preferred, which needs further exploration in the device fabrication.

Subsequently, another HSQ planarization is performed to form an isolation spacer between the gate metal and top contact deposited later. This step should calibrate carefully for the spacer thickness. Typically, the top 30 nm of the nanowires is exposed for the top contact. 6 nm Ni sputtering and lift-off process are conducted. For Ge samples, NiGe metallization is formed by FGA at 400 ℃ for 30s, while for GeSn devices, FGA is done at 325 ℃ for 10s. The annealing parameters are determined for low contact resistance. Later on, contact vias are defined by CHF_3 dry etching through HSQ planarization film to get access to the buried

gate and bottom region. Note that the TiN gate surface is 40 nm higher than the bottom plane, in order to expose the bottom region, TiN metal would be over-etched by CHF_3. However, from the TEM observation, TiN metal remains intact after etching. Finally, the devices end with 10 nm Ti/200 nm Al metal by sputtering and lift-off processes, followed by the post-metallization annealing at 300 ℃ for 10 mins, as shown in Fig. 4.1 (f).

With the well-developed process flow, vertical nanowire pMOSFETs based on undoped Ge and Ge p^+-p^--p^+ doping profile have been demonstrated in sessions 4.2 and 4.3. The systematical study of electrical properties gains an insight into vertical Ge nanowire pMOSFETs and points out the plausible methods as performance boosters. It naturally leads to the introduction of GeSn material and the following work of GeSn/Ge nanowire transistors in session 4.4.

4.2. Vertical nanowire pMOSFETs based on undoped Ge

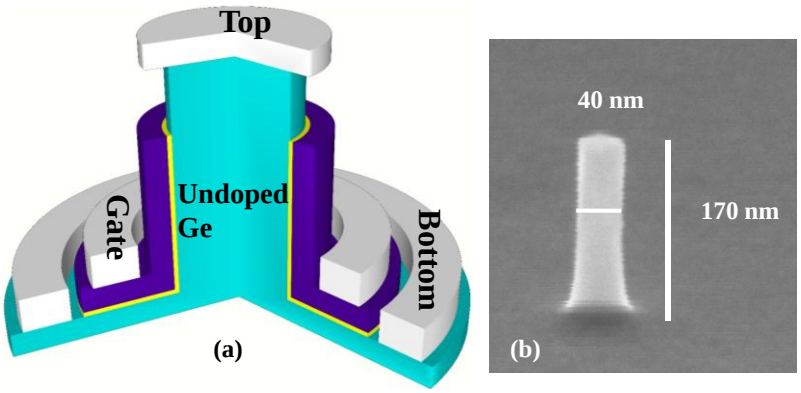

Fig. 4.2 (a) 3D schematic of a single vertical nanowire pMOSFET based on undoped Ge. This device displays no doping junction with a background doping concentration of ~3×10^{16} cm^{-3} during growth. (b) SEM image of undoped Ge nanowire with a diameter of 40 nm and a height of 170 nm.

The first tryout of vertical nanowire pMOSFETs is conducted with undoped Ge material (Here "undoped" means no additional doping except the background during CVD growth). The device fabrication follows the process flow in session 4.1. The 3D schematic of the fabricated device is shown in Fig. 4.2 (a), this device displays no junction for the doping. In reality, the background doping concentration is ~3×10^{16} cm^{-3}. Fig. 4.2 (b) is the SEM image of undoped Ge nanowire with a diameter of 40 nm and a height of 170 nm. The I_{DS}-V_{GS} transfer characteristics of a single Ge nanowire pMOSFET is shown in Fig. 4.3 (a), I_{ON} is low at both drain bias of -0.1V and -0.5V, the I_{ON}/I_{OFF} ratio is only 2 orders of magnitude,

indicative of Schottky contacts. This is confirmed by the I_{DS}-V_{DS} output characteristics in Fig. 4.3 (b) with a typical super-linear turn-on property. What is more, by measuring the *I-V* characteristics in two bottom contacts for two adjacent devices as shown in Fig. 4.4 (a), it also shows the Schottky contact behavior. Although strong Fermi level pinning close to the valence band edge leads to a small Φ_B for holes, large tunneling distance across the Schottky barrier for undoped Ge still impedes Ohmic contact formation. To alleviate this issue, heavy p-type doping in Ge layers is still required.

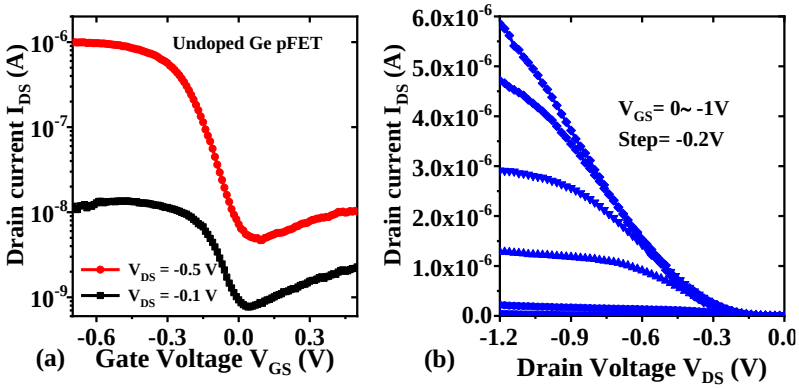

Fig. 4.3 (a) I_{DS}-V_{GS} transfer characteristics of a single undoped Ge GAA nanowire pMOSFET with a diameter of 40 nm at V_{DS} of -0.1V and -0.5V. The I_{ON} is low at both drain biases and the I_{ON}/I_{OFF} ratio is about 2 orders of magnitude. (b) I_{DS}-V_{DS} output characteristics showing typical super-linear turn-on property. This means the contacts for the devices are Schottky contacts due to the undoped Ge layers.

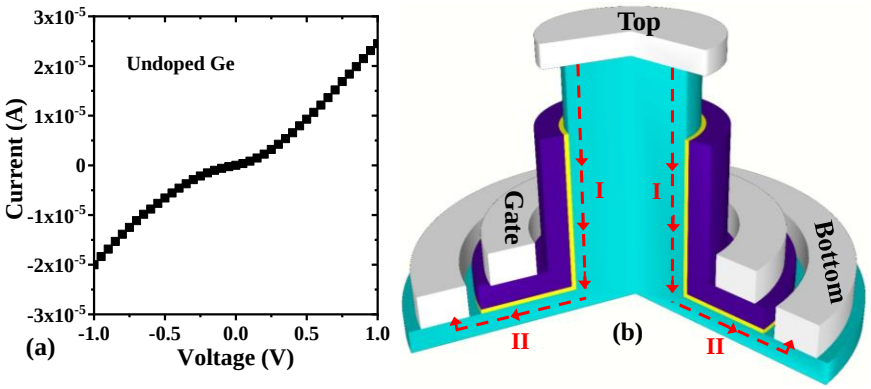

Fig. 4.4 (a) *I-V* curve in two bottom contacts for two adjacent devices, showing Schottky contact behavior. (b) Current paths for undoped Ge nanowire pMOSFET. The channel components consist of Path I in the nanowire and Path II in the planar region.

Fig. 4.4 (b) shows the current paths for undoped Ge nanowire pMOSFETs, since there are no doping junctions, the channel components are not only in the vertical nanowire direction (Path

I) but also in the planar region underneath the gate stack (Path II). Here it gives rise to the issue of gate alignment towards source/drain for vertical nanowire transistors since it is not a self-aligned process compared to FinFETs and horizontal nanowire transistors. As is similar to the undoped case shown above, junctionless-mode with heavy doping is particularly promising for applications in vertical nanowire transistors. However, it also faces the same alignment problems by the structure because the channel part is determined by the gate position. Therefore, the structure shown in Fig. 4.4 (b) needs the improvement with the bottom spacer isolation between the gate stack and bottom plane, which will cut off the channel path II in the planar region. Then the physical channel length will be determined by the top gate stack recess process. Furthermore, for vertical nanowire devices with inversion-mode or heterojunctions, the alignment is also crucial. The device simulation shows that the variation in the gate alignment towards source/drain, resulting in underlap or overlap at the source/drain would induce the possible I_{ON} loss and I_{OFF} increase [206]. Therefore, precise control of gate position and length is essential for high-performance vertical nanowire transistors.

4.3. Vertical nanowire pMOSFETs based on Ge p^+-p^--p^+ doping

As shown in the previous session, an appropriate doping profile for Ge nanowire pMOSFETs is indeed advantageous to improve electrical performance not only by the formation of excellent Ohmic contacts but also by the reasonable gate alignment. In this session, p^+-p^--p^+ doping profile in the Ge stacks along the nanowire direction is adopted to achieve this purpose. The Ge:B / Ge / Ge:B stack is grown with GeH_4 and B_2H_6 [207]. The ECV measurement shown in Fig. 4.5 (a) indicates an active Boron doping concentration of ~ 3×10^{19} cm^{-3} in the top/bottom epi-stacks and unintentionally p-type doping with ~ 3×10^{17} cm^{-3} in the middle layer due to the memory effect. In this case, the designed devices using this material stack work in the accumulation-mode, and the channel length is determined by the thickness of the light doping stack. What is practical is that the channel with light doping is easy to be depleted by the GAA gate, which can afford a wide nanowire diameter range, therefore it provides the possibility for the study of nanowire diameter scaling in the following session.

The device fabrication is the same as that of undoped Ge devices, as presented in session 4.2. After digital etching, the smallest nanowire with a diameter of 20 nm is presented with an SEM image in Fig. 3.9 (b). The conformal gate stack with $TiN/Al_2O_3/GeO_x$ is shown in Fig. 3.14. After HSQ planarization, top gate stack recess, and contact formation, the fabricated

device is displayed in Fig. 4.6 (a) with a cross-sectional TEM image, showing multi-layer stacks consisting of top and gate contacts (bottom contact cannot be seen here), separated by HSQ planarization spacer. Note that a slight wave effect close to the top of the nanowire is observed, further improvement on the planarization is required. Fig. 4.6 (b) shows a top-view SEM image of the fabricated Ge nanowire pMOSFET with bottom, gate, and top contacts, which corresponds to the 3D schematic shown in Fig. 4.5(b).

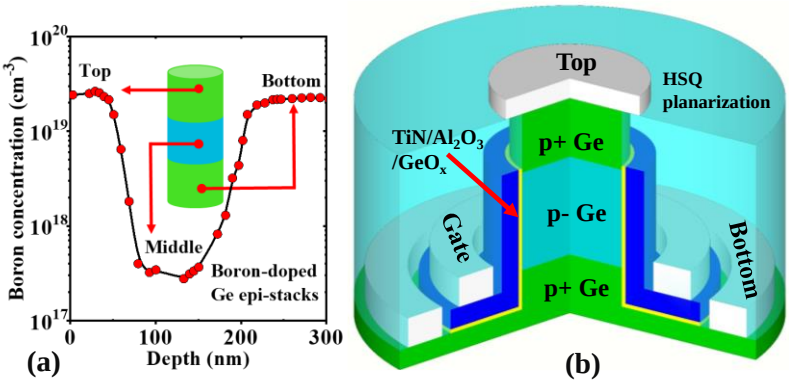

Fig. 4.5 (a) ECV measurement of active Boron doping concentration in the epi-stacks along the nanowire. The top/bottom Ge layers show ~ 3×10^{19} cm^{-3} p-type doping. (b) 3D schematic of a single vertical nanowire pMOSFET based on Ge p^+-p^--p^+ doping. High-κ Al_2O_3 is applied, and HSQ is used for device planarization.

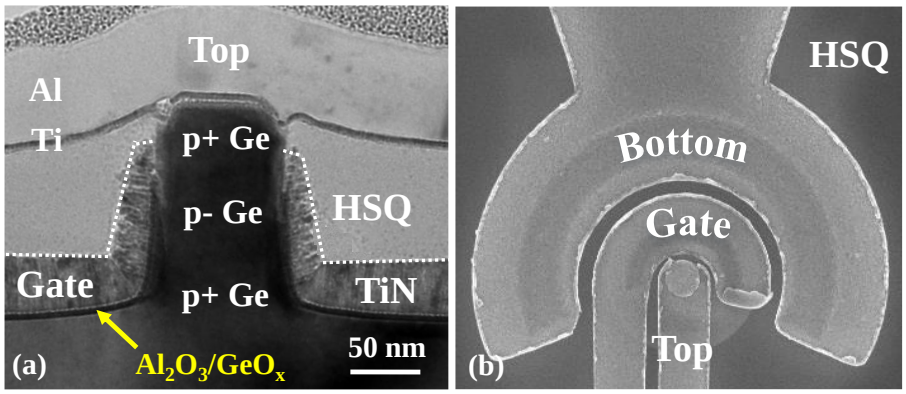

Fig. 4.6 (a) Cross-sectional TEM image of a vertical Ge nanowire pMOSFET with TiN/Al_2O_3/GeO_x gate stack and contacts, separated by HSQ planarization spacer. FIB cut by Elmar Neumann, Helmholtz Nano Facility and TEM by Jin Hee Bae, PGI-9, Forschungsentrum Juelich. (b) Top-view SEM image of the fabricated Ge nanowire pMOSFET, showing bottom, gate, and top contact, which corresponds to the 3D schematic shown in Fig. 4.5(b).

4.3.1. I-V characterization

The fabricated devices are characterized at room temperature with a PA 300 semi-automatic probe system and a Keithley 4200 semiconductor parameter analyzer. In the layout, all of the fabricated vertical Ge nanowire pMOSFETs have the same channel length since it is determined by the material growth. And transistors with various diameters are designed and fabricated. Thanks to the reproducible process, many working devices are obtained on the same chip, therefore studies of dependence of electrical FOMs, e.g. *SS*, $G_{m,ext}$, R_{tot} on (i) nanowire diameter scaling, (ii) source/drain asymmetry, and (iii) low temperatures are carried out, which will be presented in the following sessions.

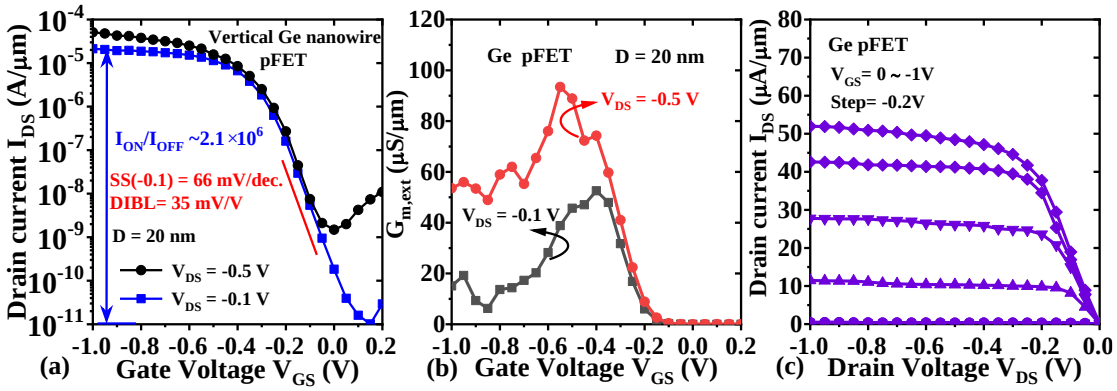

Fig. 4.7 (a) I_{DS}-V_{GS} transfer characteristics of a single vertical Ge nanowire pMOSFET with a 20 nm diameter: low SS of 66 mV/dec, small DIBL of 35 mV/V and an I_{ON}/I_{OFF} ratio of 2.1×10^6 at V_{DS} = -0.1V. The measurement is in TCD configuration. (b) The peak extrinsic transconductance $G_{m,ext}$ versus V_{GS} at V_{DS} of -0.5V and -0.1V. (c) I_{DS}-V_{DS} output curves of the corresponding Ge pMOSFET at V_{GS} from 0 to -1V, showing excellent current saturation. The I_{DS} achieves ~52 μA/μm at V_{GS}= V_{DS} = -1V.

Fig. 4.7 shows the representative electrical characteristics of the device with a diameter of 20 nm. The gate length is 150 nm and *EOT* = ~5nm. Throughout this work, the drain currents are normalized to the nanowire perimeters (π × diameter). In planar transistors, FinFETs and horizontal nanowire devices, source and drain are symmetrical in terms of their physical structures. Whereas, for vertical nanowire architectures, there is an inherent asymmetry between source and drain due to the difference in contact areas. Therefore, the devices can be measured by top-contact as the drain (TCD) configuration or top-contact as the source (TCS) configuration. Fig. 4.7 (a) depicts I_{DS}-V_{GS} transfer characteristics with TCD configuration. Due to the excellent gate electrostatic integrity provided by the 3D GAA nanowire architecture, the post-oxidation passivation method and NiGe contacts, low *SS* of

66 mV/dec, small DIBL of 35 mV/V, and a high I_{ON}/I_{OFF} ratio of ~2.1×10^6 at V_{DS} = -0.1V are obtained. It is noted that *SS* is extracted as the average slope over two orders of magnitude of I_{DS}. The peak extrinsic transconductance $G_{max,ext}$ is ~95 µS/µm and ~ 50 µS/µm at V_{DS} = -0.5V and -0.1V, respectively in Fig. 4.7 (b).

The corresponding I_{DS}-V_{DS} output curves are shown in Fig. 4.7 (c) with good saturation properties. I_{DS} achieves ~52 µA/µm at V_{GS}= V_{DS} = -1V. The low on-state current is attributed to the large total resistance R_{tot} for the 20 nm diameter nanowire pMOSFET, which is calculated to be 16 kΩ·µm at V_{GS} -V_{TH} = V_{DS} = -0.5V (The threshold voltage V_{TH} is determined at 100 nA/µm). This is much larger than the extrinsic resistance target (300 Ω·µm) required by the International Roadmap for Devices and Systems (IRDS-2017). In the vertical nanowire architecture, indeed, the top contact covers only a small nanowire tip while the bottom contact sits on a large conductive plane. Therefore, R_{tot} is primarily dominated by the top contact resistance, which results in a challenging bottleneck to scale nanowire diameters to a small dimension. This issue needs to be tackled properly facing all of group III-V and IV vertical nanowire transistors. [100, 208-209].

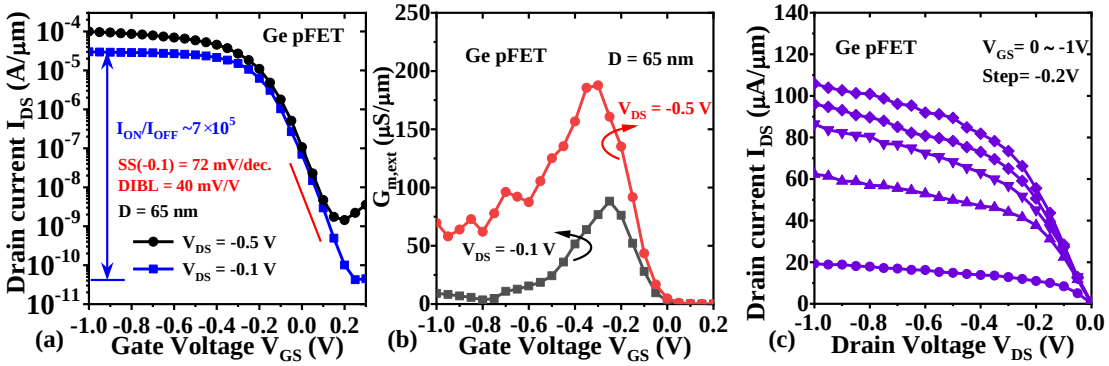

Fig. 4.8 I_{DS}-V_{GS} characteristics (a), $G_{m,ext}$ versus V_{GS} (b), and I_{DS}-V_{DS} output curves (c) of a Ge nanowire pMOSFET with a 65 nm diameter: low *SS* of 72 mV/dec, small DIBL of 40 mV/V and an I_{ON}/I_{OFF} ratio of ~7×10^5 at V_{DS} = -0.1V. The maximum $G_{m,ext}$ is ~ 190 µS/µm at V_{DS} = -0.5V.

As is reported in the literature, several novel processing strategies have been proposed to further improve the contact resistance for ultra-scaled vertical nanowire transistors: (i). Increasing the doping concentration of the top/bottom epi-stacks by non-equilibrium methods to promote dopant activation in Ge, e.g. flash lamp annealing or laser annealing, would result in small contact resistance, a small R_{tot} and therefore an enhanced I_{ON}. [192-193, 210]; (ii). Epitaxial growth on top of the nanowire or a gate-last process aimed at increasing the top contact area is one plausible option to reduce the top contact resistance [211]; (iii). Arrays of

nanowire transistors are also a performance booster for reduced parasitic capacitances and improved current drivability [100, 211].

Similarly, Fig. 4.8 (a-c) show decent electrical results for a 65 nm diameter nanowire Ge pMOSFET, in which *SS* of 72 mV/dec, DIBL of 40 mV/V, and an I_{ON}/I_{OFF} ratio of ~7×10^5 at V_{DS}= -0.1V are obtained. The maximum $G_{m,ext}$ is ~ 190 µS/µm at V_{DS} = -0.5V. In this work, the adopted 3D GAA nanowire architecture is greatly beneficial for the excellent subthreshold characteristics as is discussed above. The presented *SS* and DIBL values are essentially comparable to the state-of-the-art Ge pFinFETs and horizontal Ge GAA nanowire pMOSFETs [57-66]. The I_{ON}/I_{OFF} ratio at higher V_{DS} is degraded, which can be attributed to the gate-induced drain leakage (GIDL) effect in Ge devices. Considering Ge owns a small bandgap (~ 0.65 eV), BTBT assisted leakage currents become prominent. Hence, bandgap engineering, e.g. introducing heterostructures with larger bandgap Si or SiGe in the drain side, contributes to suppressing leakage current and thus increase I_{ON}/I_{OFF} ratio.

From the output characteristics comparison in Fig. 4.7 (c) and Fig. 4.8 (c) for Ge nanowire transistors with diameters of 20 nm and 65 nm, the output saturation properties for the 20 nm nanowire device are much better than that for 65 nm nanowire device, which can be evaluated employing the output conductance G_d:

$$G_d = \frac{\partial I_d}{\partial V_d} \tag{4.1}$$

This means G_d (20 nm) is smaller than G_d (65 nm). Typically, G_d becomes zero as the devices operate in the saturated region, which is an important FOM in analog circuit design. As is stated in the 20 nm nanowire device, the top drain contact resistance is very large, contributing to a large drain resistance R_D and total resistance R_{tot}, therefore, the voltage drop on R_D is also large. The first-order relationship among R_D, $I_{DS,}$ and V_{DG} in a MOSFET can be written as:

$$V_{DG,int} = V_{DG} - I_{DS} \times R_D \tag{4.2}$$

Where $V_{DG,int}$ is the intrinsic drain-to-gate voltage, which determines the pinch-off property in the output characteristics. The drain current pinches off when $V_{DG,int}$ = -V_{TH}. This means that a large R_D results in a reduction of $V_{DG,int}$, impeding the saturation property in a transistor. What is more, short-channel effects should be taken into account for devices with various diameters. As a consequence, 20 nm nanowire devices have a better saturation behavior compared to 65 nm devices and it well explains G_d (20 nm) < G_d (65 nm).

Mobility extraction

The field carrier mobility μ is used to characterize how fast the carrier moves through a semiconductor under the applied electric field. Generally, carrier mobility in MOSFETs is lowered due to the strong surface roughness scattering compared to bulk mobility. Here, in the linear regime of a transistor, the effective carrier mobility μ_{eff} can be approximately extracted as [212]:

$$\mu_{eff} = \frac{G_m L_g^2}{C_{ox} V_{DS}} \tag{4.3}$$

Where L_g is the channel length. Noted that C_{ox} is very small for ultra-scaled nanowire transistors and challenging to be measured. Therefore, the theoretical calculation of C_{ox} by the cylinder capacitor model is used for GAA structures:

$$C_{cylinder} = \frac{2\pi\varepsilon_0\varepsilon_{ox} L_g}{ln(b/r)} \tag{4.4}$$

Where r is the radius of the Ge nanowire, d is the dielectric thickness, then $b = r + d$.

By substituting the experimental values into the above equation for the 20 nm diameter nanowire pFET, the extracted effective hole mobility μ_{eff} is ~75 cm^2/V s. This value is to some degree underestimated, setting a minimum limit, because these simplified equations do not exclude the effect of external source/drain series resistance. Further precise mobility extraction in nanowire transistors should be considered.

4.3.2. Nanowire diameter scaling

The geometric scaling in a transistor e.g. gate length, width, or oxide thickness has been long pursued and is essential to improve device performance generation by generation. Regarding the vertical nanowire transistors, the straightforward scaling component is nanowire diameters, thus, various nanowire dimensions ranging from 65 nm to 20 nm in the layout are designed. The study of nanowire diameter dependency relies on high device reproducibility with well-behaved electrical properties. In this session, the data points are measured based on ~20 functional devices under the same fabrication and measurement conditions.

The key electrical FOMs for Ge nanowire pMOSFETs with various diameters are summarized in Fig. 4.9. The mean value is shown to represent each data point. Fig. 4.9 (a) shows *SS* scaling metrics as a function of diameters. Mean *SS* values for 20 nm and 45 nm nanowire devices exhibit less than 70 mV/decade, proving excellent gate electrostatic controllability. As nanowire diameter is scaled from 65 nm to 45 nm, *SS* shows a decaying

trend as expected. However, when the nanowire diameter is shrunk to 20 nm, devices show slightly higher mean *SS* and more spreading data compared to 45 nm nanowire devices. This is probably due to the following reasons: (i) As nanowire diameter shrinks, the nanowire diameter uniformity is more sensitive to the etching process variations, leading to a larger spread of *SS*; (ii) Stronger surface roughness on the smaller nanowire sidewalls could contribute to higher D_{it}, and therefore larger *SS*. Robust surface passivation methods especially for ultra-scaled nanowire transistors should then be developed. In this work, both 20 nm and 45 nm nanowire transistors can achieve the smallest *SS* value of 66 mV/dec at V_{DS} of -0.1V, demonstrating the advantage of GAA nanowire structures.

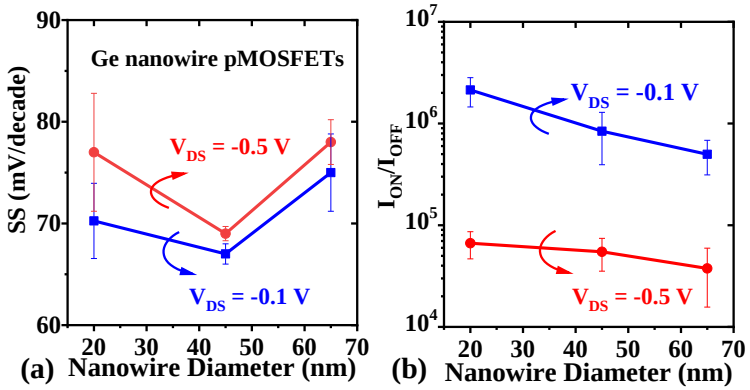

Fig. 4.9 (a) *SS* scaling metrics of Ge nanowire devices with various diameters. As nanowire diameter is scaled from 65 nm to 45 nm, *SS* shows a decaying trend as expected. However, further diameter scaling to 20 nm results in a slightly higher mean SS primarily due to the nanowire diameter variation, surface roughness, and D_{it}. (b) I_{ON}/I_{OFF} ratio versus various nanowire diameters. The smallest nanowire devices have the largest I_{ON}/I_{OFF} ratio due to the strongest gate electrostatics.

The I_{ON}/I_{OFF} ratio as a function of nanowire diameters is presented in Fig. 4.9 (b). Due to the current transportation in the vertical direction, it completely cut off the parasitic leakage paths from the bulk compared to the planar devices. Along with 3D nanowire geometry, the device is easy to turn off, beneficial for suppressing subthreshold leakage. Therefore, the vertical Ge nanowire pMOSFETs exhibit high I_{ON}/I_{OFF} ratios, which increases as the nanowire diameter scales down at both V_{DS} of -0.1 V and -0.5 V. Maximum I_{ON}/I_{OFF} ratios of ~2.3×10^6 at V_{DS} of -0.1V are obtained for the smallest nanowire transistors. EOT in these devices is ~ 5 nm, which is quite large. Scaling EOT is reasonable to improve *SS*, I_{ON}, and I_{ON}/I_{OFF} ratio, which will be discussed in the following.

Another key FOM is the DIBL characteristics versus various nanowire diameters. DIBL is calculated as:

$$DIBL = -\frac{V_{TH}^{H} - V_{TH}^{L}}{V_{DD}^{H} - V_{DD}^{L}} \tag{4.5}$$

Where V_{TH}^{H} is the threshold voltage measured at the high supply voltage V_{DD}^{H} and V_{TH}^{L} is the threshold voltage at a low voltage V_{DD}^{L}. Here in this work, V_{DD}^{H} and V_{DD}^{L} are -0.5V and -0.1V, respectively. Note that the threshold voltage V_{TH} is determined at 100 nA/µm. As the nanowire diameter decreases, DIBL exhibits a decreasing trend, demonstrating better immunity against short-channel effects (cf. Fig. 4.10 (a)). All of the DIBL values are well kept below 51 mV/V, and DIBL for the largest nanowire devices shows a mean value of 39 mV/V.

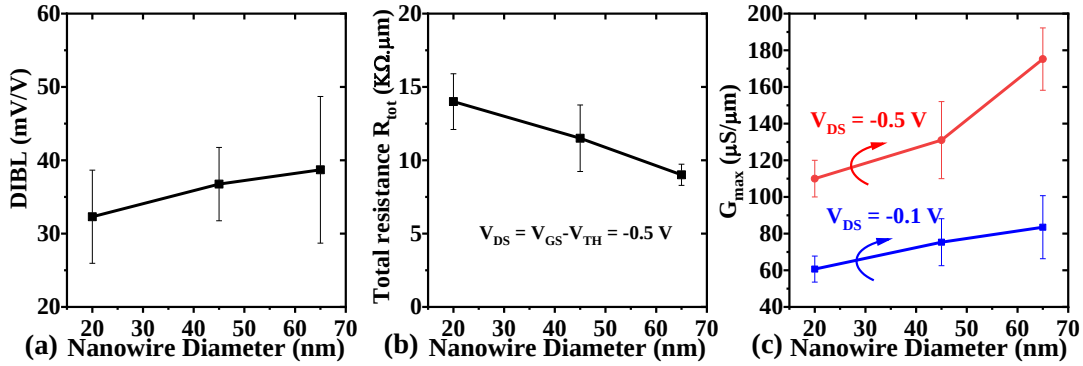

Fig. 4.10 (a) DIBL scaling as a function of nanowire diameters. As the nanowire diameter decreases, DIBL exhibits a decreasing trend, demonstrating better immunity against short-channel effects. (b) R_{tot} scaling properties with various nanowire diameters. R_{tot} increases from 9 kΩ·µm up to 14 kΩ·µm as the nanowire diameter decreases from 65 nm down to 20 nm. (c) Peak G_{max} versus nanowire diameters measured at V_{DS}= -0.1V and -0.5V. Larger diameter nanowire devices show higher G_{max} due to smaller total resistance R_{tot}.

Furthermore, to improve the on-state performance for transistors, total resistance R_{tot} has to be lowered. Generally, R_{tot} consists of contact resistance, channel resistance, etc., which can be simply extracted from the I_{DS}-V_{GS} transfer curves by using V_{DS}/I_{DS}. In Fig. 4.10 (b), R_{tot} increases from 9 kΩ·µm up to 14 kΩ·µm extracted at $V_{DS} = V_{GS} - V_{TH}$ = -0.5V as the nanowire diameter decreases from 65 nm down to 20 nm, displaying an obvious diameter dependency. Because the top contact resistance depends on the contact areas with various nanowire diameters. The tiny top contact area associated with a small nanowire leads to a large contact resistance, which contributes to a large part of $R_{tot,}$ especially in smaller nanowire transistors. Novel solutions have been proposed in session 4.3.1. Conversely, it can be easily speculated that I_{ON} would raise as nanowire diameter is increased (not shown here).

Contrary to R_{tot} dependence on nanowire diameters, the peak transconductance G_{max} decreases as the nanowire diameter drops at both V_{DS} of -0.1V and -0.5V (cf. Fig. 4.10 (c)). This can be explained that larger R_{tot} significantly degrades extrinsic $G_{m,ext}$, and consequently smaller G_{max} are obtained. Such reports were also observed in vertical III-V nanowire nMOSFETs [208].

4.3.3. Source/drain asymmetry

So far, the electrical characteristics for vertical Ge nanowire pMOSFETs are only concerned with TCD configuration in previous sessions. However, due to the asymmetrical top/bottom contacts, TCS configuration should be also taken into account to study the performance difference, which would serve as the guidelines for circuit design. Therefore, electrical measurement with both configurations is conducted and detailed performance comparison is discussed here.

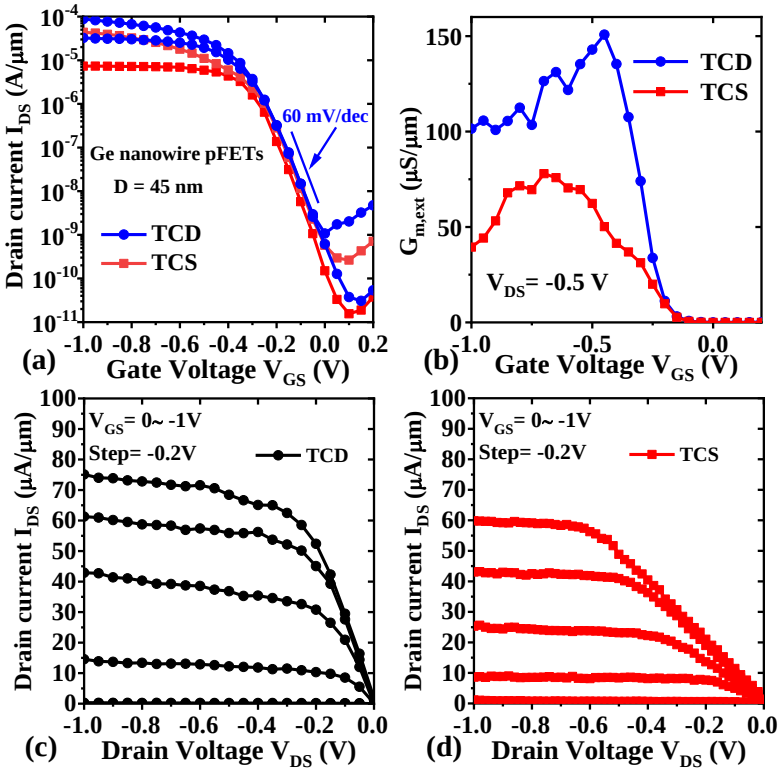

Fig. 4.11 Performance comparison of an exemplary 45 nm diameter nanowire pMOSFET with TCD and TCS configurations with (a) I_{DS}-V_{GS} transfer characteristics. Both I-V curves show similar subthreshold properties. (b) $G_{m,ext}$ characteristics at V_{DS} = -0.5V. The peak $G_{m,ext}$, ~151 μS/μm for TCD configuration, is larger than that for TCS configuration (78 μS/μm). (c-d) I_{DS}-V_{DS} output characteristics for both measurements. In the linear region, the slope with TCS configuration is smaller than that with TCD configuration.

An exemplary 45 nm diameter nanowire pMOSFET with TCD and TCS configurations is applied to investigate the impact of source/drain swapping. I-V transfer characteristics with both configurations are shown in Fig. 4.11(a). It is seen that the subthreshold characteristics for both measurements barely change. The *SS* keeps quite small and exhibits similar values. Indeed, *SS* calculation in this case, should take the external series resistance into account, namely, source resistance R_S:

$$SS = \frac{d(V_{GS})}{d(lgI_{DS})} = \frac{d(V_{GS,int})}{d(lgI_{DS})} + \frac{d(R_S I_{DS})}{d(lgI_{DS})} = SS_{int} + R_S I_{DS} ln10 \quad (4.6)$$

Where V_{GS} is divided into intrinsic gate voltage $V_{GS,int}$, and the voltage drop across R_S (R_S $\times I_{DS}$). R_S is source series resistance and SS_{int} is the intrinsic *SS*.

From Equation 4.6, *SS* is not only consisting of the intrinsic SS_{int}, but also R_S contribution by R_S $\times I_{DS}$ $\times$ln10. While I_{DS} is very small in the subthreshold region, the second part of *SS* will contribute negligibly. This explains why *SS* does not change distinctly for the device with both configurations. It is also confirmed the advantage of GAA nanowire geometry adopted in this work. Besides, it is interesting to note that as I_{DS} continues to increase at the shoulder regime in the I_{DS}-V_{GS} curves, the *SS* changes appreciably, and the saturation property of I_{ON} is also affected, this is because R_S $\times I_{DS}$ cannot be ignored since I_{DS} is large.

What is more, the V_{TH} with TCS configuration shows a negative shift compared to that with TCD configuration in Fig. 4.11 (a). As explained previously, due to the contact area asymmetry, source series resistance R_S in the TCS configuration is far larger than the drain resistance R_D ($R_S >> R_D$), while in the TCD configuration, $R_D >> R_S$. Thereby, part of V_{GS} drops across the R_S in the TCS configuration, giving rise to a negative shift of V_{TH} compared to the device with TCD configuration. In addition, the transistor with TCS configuration exhibits slightly larger DIBL than that with TCD configuration.

The asymmetry in I_{ON} properties for both configurations can be observed in I_{DS}-V_{GS} curves. The I_{ON} with TCD configuration is larger than that with TCS configuration, which can be attributed to the difference in R_{tot}. It can also be reflected in peak $G_{m,ext}$ properties as shown in Fig. 4.11 (b), the difference of peak $G_{m,ext}$, which is ~151 µS/µm for TCD configuration and ~78 µS/µm for TCS configuration at V_{DS} = -0.5V, is attributed to the R_S/R_D asymmetry since $G_{m,ext}$ is primarily related to R_S part [213].

From the above discussions, the significant difference in key FOMs for vertical nanowire transistors with both configurations can be mostly attributed to the asymmetry of R_S and R_D. Thus, it is imperative to investigate what is the fundamental cause of resistance differences in vertical nanowire structures. Firstly, contact area diversity in the top/bottom contacts can

directly lead to the R_S/R_D difference, however, this cannot entirely elucidate R_{tot} asymmetry. Other than this, the contact resistivity should be considered thoroughly. It was demonstrated that the ionization energy of dopants in the nanowire increases as the nanowire diameter decreases, resulting in a doping deactivation effect and consequently a lowered active doping concentration, especially in ultra-scaled nanowires [214]. It is said that the dielectric mismatch between the nanowire and its surroundings is responsible for this effect. In this case, the active doping concentration on the top nanowire region where top contact forms might degrade, forming a not perfect Ohmic contact, this means, carrier tunneling and thermionic emission both contribute to the contact despite Fermi level pinning close to the valence band edge. Therefore, it is reasonable to deduce that the Schottky tunneling barrier width across the contact can be partially modulated by the applied voltage, leading to voltage-dependent contact resistivity and resistance. Moreover, the contact resistivity could be affected by quantum confinement and surface segregation of dopants exclusively at nanowire diameter below 10 nm [215]. This provides practicable hints for the future sub-10 nm diameter nanowire transistors.

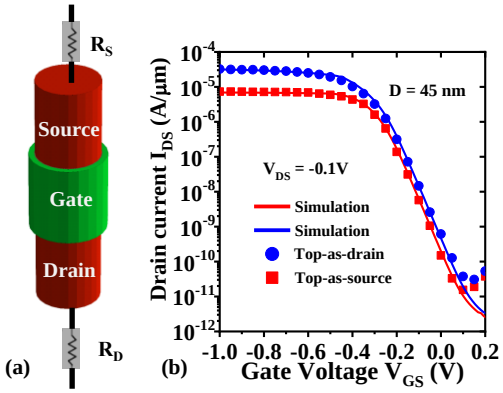

Fig. 4.12 (a) Schematic of a simulated nanowire structure with external resistors. For simplicity, the external equivalent resistors in the source and drain side are used to imitate R_S and R_D. (b) The simulated and experimental transfer curves for 45 nm nanowire pMOSFETs with TCS and TCD configurations at V_{DS}= -0.1V. The R_S/R_D ratio can be extracted from the good agreement between the fitting and experimental data, which are ~12:1 and ~1:4 for TCS and TCD configurations, respectively.

Indeed, this hypothesis is directly sustained by electrical characterization. In the TCS configuration, the top source contact is connected to the ground potential, while the top drain contact in the TCD configuration is connected to the high drain bias. As a consequence, the top contact resistivity in the TCS configuration is larger than that in TCD configuration, so is the contact resistance. This can also explain R_{tot} difference very well. Apparently, the I_{ON}

asymmetry can be concluded. Fig. 4.11 (c-d) depict the I_{DS}-V_{DS} curves with TCS and TCD configurations. In the linear region, the slope with TCS configuration is smaller than that with TCD configuration due to the larger R_{tot} in the device with TCS configuration. This also leads to the delayed current saturation in the TCS configuration.

From the above analysis, it is known that R_S/R_D and R_{tot} asymmetry exist in vertical nanowire transistors. It would be reasonable to gain the physical intuition of what is the proportion of R_S or R_D in R_{tot}. However, from experimental results, it cannot be extracted specifically. Therefore, device simulation is carried out by Sentaurus Technology Computer-Aided Design (TCAD) [216], through fitting the electrical curves, R_S or R_D can be estimated. Here the physical parameters of the fabricated nanowire devices, e.g. doping, gate length, diameter, are applied into the simulation. Fig. 4.12 (a) is the simulated nanowire structure with external resistors. For simplicity, the external equivalent resistors in the source and drain side are used to imitate R_S and R_D. Fig. 4.12 (b) shows the simulated and experimental transfer curves for 45 nm nanowire pMOSFETs with TCS and TCD configurations at V_{DS}= -0.1V. The R_S/R_D ratio can be extracted from the good agreement between the fitting and experimental data, which are ~12:1 and ~1:4 for TCS and TCD configurations, respectively. These values are consistent with the R_S/R_D asymmetry in the experiments. The obtained R_S/R_D ratio with TCD configuration is similar to that (~1:5) in the vertical III-V nanowire transistors also with top-as-drain configuration [217].

To apply the derived R_S/R_D, it would be logical to determine the intrinsic electrical properties correcting for the asymmetric case in this work, namely intrinsic $G_{m,int}$. $G_{m,int}$ is given by [213]:

$$G_m^0 = \frac{G_{m,ext}}{1 - R_S \times G_{m,ext}} \tag{4.7}$$

$$G_{m,int} = \frac{G_m^0}{1 - R_{SD} \times G_D \times (1 + R_S \times G_m^0)} \tag{4.8}$$

Where R_S is the source series resistance, R_{SD} is the source and drain series resistance, which can be extracted by the extrapolation from transfer characteristics, G_D is the measured drain conductance and can be obtained from the output characteristics.

From the R_S/R_D ratio and R_{tot}, R_S can be estimated for both configurations. After substituting these values into the equations, $G_{m,int}$ can be obtained. However, the calculated $G_{m,int}$ is very sensitive to the R_S/R_D ratio. A minor change of R_S/R_D ratio (for example 10%) can give a large $G_{m,int}$ difference, leading to unreliable data. Therefore, more robust and accurate methods should be developed to extract the intrinsic properties for vertical nanowire transistors.

The impact of source/drain swapping on the key electrical FOMs for vertical Ge nanowire pMOSFETs with diameters ranging from 65 nm to 20 nm is investigated in Fig. 4.13. In short, transistors with TCS configuration follow similar diameter scaling trends in the key electrical FOMs compared to those with TCD configuration. However, they show a performance asymmetry for both configurations, which is proved to be inherent to vertical nanowire transistors. This general phenomenon needs to be considered in the applications that rely on vertical nanowire architectures. Fig. 4.13 (a) shows the *SS* scaling metrics with both configurations. They display similar scaling trends as is explained in 45 nm diameter nanowire pMOSFETs. *SS* with TCS configuration also keeps small due to the advantage of GAA nanowire structures. I_{ON}/I_{OFF} ratios in the TCS configuration decrease with increasing nanowire diameters as expected and become larger compared to those with TCD configuration at V_{DS} of -0.1V and -0.5V (cf. Fig. 4.13(b)). It is speculated that larger R_{tot} in the TCS configuration results in smaller off-state current compared to devices with TCD configuration, which to some degree increases the I_{ON}/I_{OFF} ratios.

Fig. 4.13(c) compares R_{tot} scaling trend with various nanowire diameters. They show a clear asymmetry at the same nanowire diameters. R_{tot} with TCS configuration is larger compared to that with TCD configuration because of top/bottom contact resistivity differences, which is elucidated before. Besides, R_{tot} for both configurations decreases as the nanowire diameters increase due to the increased top contact area. When the diameter is 65 nm, the largest one in this work, the asymmetry becomes less obvious because the top/bottom contact areas are very large, resulting in similar R_{tot}. With the contrary trend of R_{tot}, peak G_{max} versus nanowire diameters at V_{DS}= -0.5V is shown in Fig. 4.13(d). G_{max} shows a rising trend as diameters increase. As is reasonable to understand, devices with TCD configuration exhibit larger G_{max} than those with TCS configuration.

DIBL effect also depicts asymmetry phenomenon when swapping source and drain in vertical nanowire transistors (cf. Fig. 4.13 (e)). Decreased DIBL with diameters also represents the stronger electrostatic integrity in the nanowire devices. As is stated in Equation 2.4, DIBL is related to the source/drain resistance R_{SD}. As the extracted R_{SD} in TCS configuration is larger than that in TCD configuration, therefore, DIBL in TCS configuration is larger than that in TCD configuration. In Fig. 4.13(f), V_{TH} with TCS configuration shows a negative shift compared to that with TCD configuration at the same nanowire diameter, as explained before. Nevertheless, the smallest nanowire transistors have similar V_{TH} for both configurations, here the tradeoff between the top contact resistance and gate electrostatics should be taken into account.

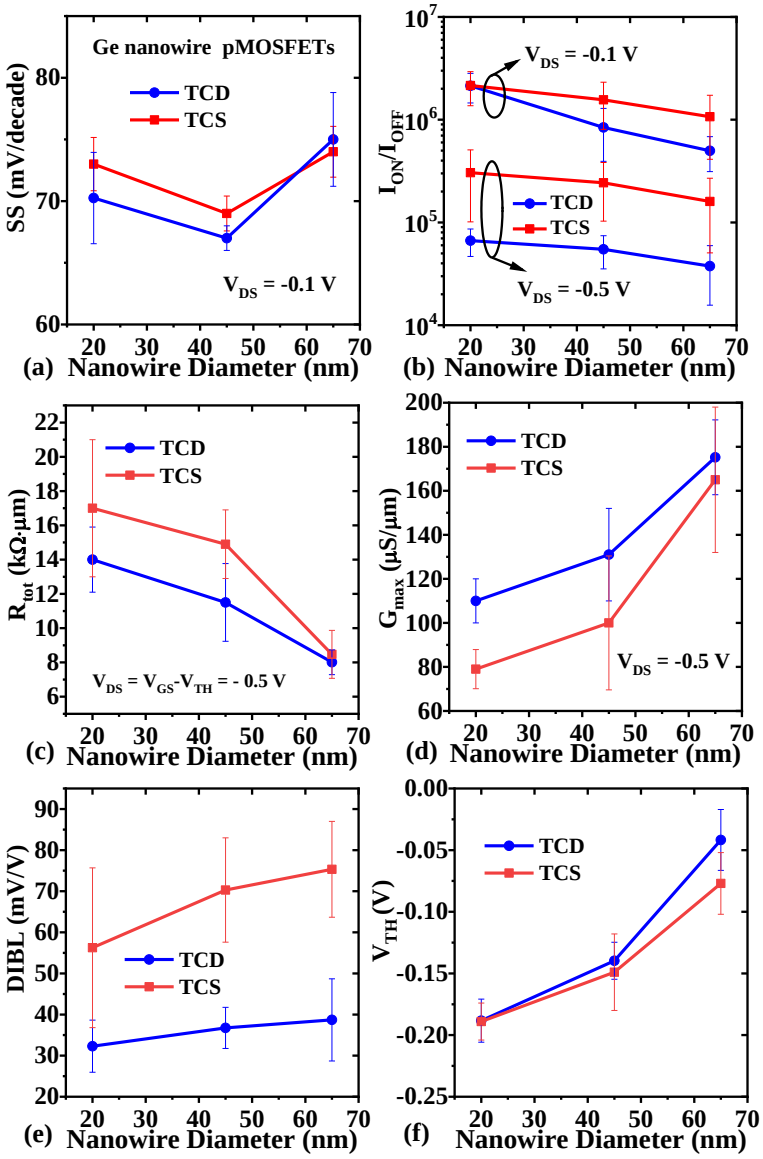

Fig. 4.13 Key electrical FOMs with source/drain asymmetry for Ge nanowire transistors: TCS vs. TCD configurations: (a) *SS* scaling metrics with various diameters at V_{DS} = -0.1V. All devices exhibit mean *SS* below 80 mV/dec. (b) I_{ON}/I_{OFF} ratios with various nanowire diameters, showing the increasing trend as the nanowire diameters scale down. (c) R_{tot} versus nanowire diameters. R_{tot} asymmetry is observed. (d) Peak G_{max} as a function of nanowire diameters measured at V_{DS}= -0.5V. Devices with TCD configuration exhibit larger G_{max} than those with TCS configuration. (e) DIBL with different nanowire diameters. DIBL with TCS configuration exhibit larger than that with TCD configuration. (f) V_{TH} scaling trend showing a negative shift in the devices with TCS configuration.

It is noteworthy in the afore-described discussions that some of the electrical FOMs for the smallest nanowire transistors show a large deviation, namely *SS*, DIBL. Several influence factors should be considered: (i) Micro-loading effect during nanowire patterning can lead to

nanowire diameter variation, thus affecting the gate electrostatics. This was also observed in the wafer-scale mapping for vertical Si nanowire transistors [206]. What is more, the variation in the specific etching parameters in nanowire patterning and digital etching steps can also lead to the diameter uniformity for small nanowires; (ii) During top gate stack recess, it is also possible to give rise to the gate length variation problems. (iii) The second HSQ planarization can cause the non-uniformity of the planarization film, resulting in the varied exposed areas for the top contact, and therefore R_{tot} variations. Significant efforts are needed to develop more robust processing in the future vertical nanowire transistor fabrication.

Benchmark

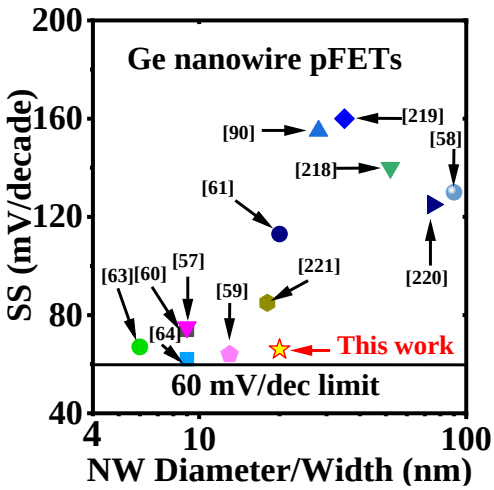

Fig. 4.14 Benchmark of *SS* with various nanowire diameters/widths among state-of-the-art Ge vertical and horizontal GAA nanowire pMOSFETs. This work demonstrates the low SS of 66 mV/decade for vertical Ge nanowire pFETs.

Fig. 4.14 benchmarks *SS* with various nanowire diameters or widths among the Ge vertical and horizontal GAA nanowire pMOSFETs reported in the literature. With optimized process modules and 3D nanowire geometry, this work successfully demonstrates high-performance vertical GAA nanowire pMOSFETs. The devices achieve low *SS* of 66 mV/decade, which is comparable to those *SS* values in the state-of-the-art horizontal 6 nm and 13 nm diameter nanowire Ge pMOSFETs, which are fabricated by the industry [59, 63-64]. Although the on-state performance in this work is not competitive with them, there is a great space to work on the source/drain engineering for vertical Ge nanowire transistors, which opens up the following study on GeSn/Ge nanowire transistors.

4.3.4. Temperature-dependent measurements

In order to investigate the underlying physical mechanisms regarding carrier transport in nanowire transistors, this part presents the low-temperature characterization on vertical Ge nanowire pMOSFETs. The dependence of key FOMs, e.g. I_{ON}, V_{TH}, *SS* on low temperatures are discussed.

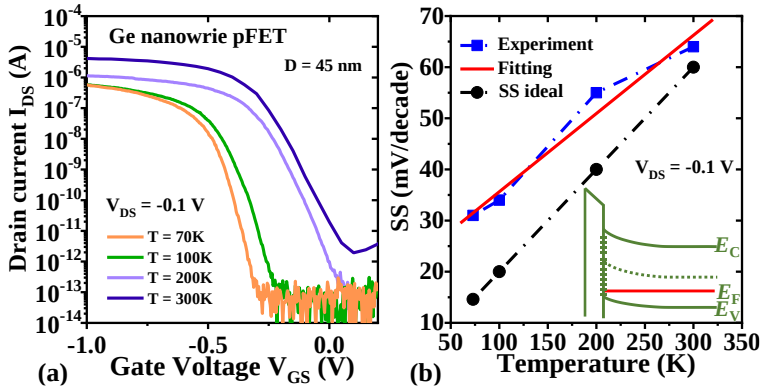

Fig. 4.15 (a) The experimental I_{DS}-V_{GS} transfer characteristics for Ge nanowire pMOSFET with a diameter of 45 nm. The temperatures vary from 300K down to 70K. With lowering temperatures, I_{ON} becomes surprisingly smaller. (b) The temperature dependence of SS characteristics. By fitting the experimental *SS* values, a linear temperature-dependence of *SS* is obtained. The deviation between experimental data and the ideal *SS* lies in D_{it} at high-κ dielectric/channel interface. Inset: energy band diagram showing the Fermi level E_F and net charge trapped in the interface states.

The experimental I_{DS}-V_{GS} transfer characteristics for a Ge nanowire pMOSFET with a diameter of 45 nm is shown in Fig. 4.15 (a) with temperatures ranging from 300K down to 70K. The on-state performance is quite sensitive to various temperatures. With lowering temperatures, on-state currents become surprisingly smaller. According to the correlation between hole mobility and temperatures, mobility enhancement induced by reduction of the phonon scattering would be obtained with decreasing temperatures. Thereby, a higher I_{ON} would be expected. However, the source/drain resistance variation with temperatures should be practically taken into account in the fabricated devices. At low temperatures, the NiGe/Ge contact resistivity might be deteriorated, because the bandgap of Ge is increased with decreasing temperatures, this will also affect the hole Schottky barrier height Φ_B in Equation 3.4. The above factors primarily lead to larger total resistance R_{tot} and decay of drive current. In addition, it is found that $G_{m,ext}$ exhibits a decreasing trend with temperatures. Similar results have been observed in Si horizontal nanowire nMOSFETs with diameters of 6 nm [222]. Regarding the off-state behavior, as temperature decreases from 300 K to 200K, I_{OFF} is

obviously lowered due to the suppressed thermal carrier generation. At T < 100 K, it shows constant $I_{OFF} \approx \sim 3 \times 10^{14}$ A.

The temperature dependence of *SS* for 45 nm nanowire transistors is also investigated. The apparent *SS* reduction with temperatures can be seen in both Fig. 4.15 (a) and (b). In Fig. 4.15 (b), it depicts the experimental *SS* data and ideal SS_{ideal} values. At room temperature (300 K), the ideal *SS* is limited to 60 mV/decade, due to the fundamental carrier injection mechanism in MOSFETs, as is described in Equation 4.9. The subthreshold performance becomes excellent at low temperatures, achieving *SS* of 30 mV/decade at 70 K. By fitting the experimental *SS* values, a linear temperature-dependence of *SS* is obtained. The deviation between experimental data and ideal *SS* lies in D_{it} at a high-κ dielectric/nanowire channel interface and the relationship is expressed in Equation 4.10.

$$SS_{ideal} = \frac{kT}{q} ln10 \tag{4.9}$$

$$SS = \frac{kT}{q} ln10 \cdot (1 + \frac{C_D + q^2 D_{it}}{C_{ox}}) \tag{4.10}$$

Where k is the Boltzmann constant and q is the electron charge. C_{ox} and C_D is the gate oxide capacitance and depletion capacitance, respectively. $C_D \approx \varepsilon_0 \varepsilon_{Ge} \frac{\pi D^2}{4L_g}$, D is the nanowire diameter. SS_{ideal} is the ideal *SS* without considering any external effects.

However, from Equation 4.10, the temperature-dependence of *SS* needs further exploration. The slope of *SS* versus various temperatures should be larger than that of ideal *SS*, if D_{it} is not correlated with temperatures. In reality, the experimental *SS* does not show constant slope and is not necessarily larger than the ideal one shown in Fig. 4.15 (b). Except that more data should be included from low-temperature measurement, the assumption of constant D_{it} needs more evaluation. At low temperatures, the slightly enlarged bandgap of Ge and shift of Fermi level E_F can cause the re-distribution of net charges in donor-like and acceptor-like traps, thus leading to variation of D_{it} and screening of gate voltage (see the inset of Fig. 4.15 (b)). It is speculated that the change of D_{it} is also responsible for *SS* change with temperatures.

What is more, another factor that should be concerned is the deteriorated source resistance R_S in vertical nanowire devices as shown in Equation 4.6. If R_S becomes large at low temperatures, then $R_S \times I_{DS} \times \ln 10$ part cannot be neglected, and *SS* is increased. Therefore, robust surface passivation and appropriate contact metal options in vertical nanowire transistors should be developed especially for cryogenic applications.

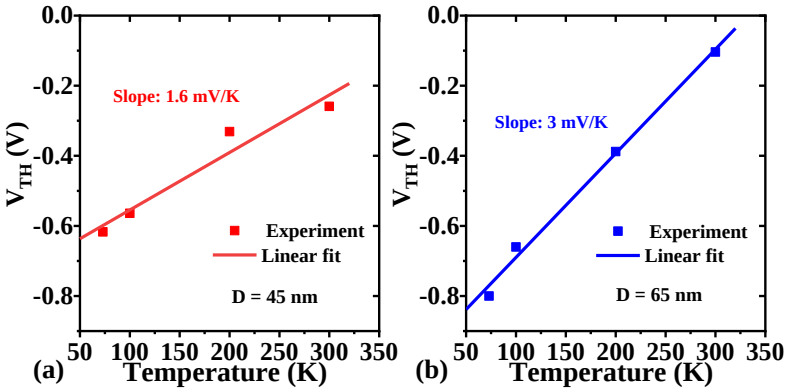

Fig. 4.16 V_{TH} versus various temperatures for Ge nanowire pMOSFETs with diameters of 45 nm (a) and 65 nm (b). It depicts a linear behavior with temperatures for both devices. Linear fitting of the data points yields a slope of 1.6 mV/K and 3 mV/K for 45 nm and 65 nm devices, respectively.

Besides *SS* trend with temperatures, the temperature-dependence of the threshold voltage V_{TH} for vertical nanowire pFETs is also discussed. An extensive study of V_{TH} has already been applied to silicon-on-insulator (SOI) and horizontal nanowire MOSFETs [219, 222-223]. The relationship between V_{TH} and temperatures can be summarized as [223]:

$$\frac{dV_{TH}}{dT} = \frac{d\emptyset_F}{dT}\left[\alpha\sqrt{\frac{q\epsilon_r N_{eff}}{\emptyset_F C_{ox}^2}} + 2 + \frac{qD_{it}}{C_{ox}}\right] \tag{4.11}$$

Where Φ_F is the Fermi potential, ϵ_r is the Ge permittivity. N_{eff} is an effective dopant concentration. α = 1 for a partially depleted channel and α = 0 for a fully depleted channel. Since in this work, the channel doping is low, and in addition to the 3D GAA geometry, the channel is fully depleted. Then α = 0, dV_{TH}/dT is a function of Φ_F, which is related to the bandgap variation. Fig. 4.16 shows the V_{TH} versus various temperatures for 45 nm and 65 nm nanowire pMOSFETs. The threshold voltage is extracted at 100 nA/μm and V_{DS} = -0.1V. It depicts a linear trend with temperatures for both devices. A linear fit of the data points yields a slope of 1.6 mV/K and 3 mV/K for 45 nm and 65 nm devices, respectively. The difference in temperature coefficients for 45 nm and 65 nm nanowire pMOSFETs is attributed to gate electrostatic control over the channel and voltage drop on R_s. For Ge horizontal nanowire transistors with a diameter of 35 nm, a slope of 1.46 mV/K was reported [219], which is consistent with the data in this work.

4.4. Vertical nanowire pMOSFETs based on GeSn/Ge

From the afore-mentioned analyses for vertical Ge GAA nanowire pMOSFEFs, one noteworthy issue is the top contact resistance in vertical nanowire transistors, specifically including a small contact area and active doping concentration. As was already suggested in session 4.3.1, here another practical way to reduce contact resistivity is provided in this part: introducing a small bandgap GeSn material as the top layer which is depicted in Fig. 4.17 (a). The principle is that the effective Schottky barrier height Φ_B at NiGeSn/GeSn is smaller than that of NiGe/Ge, contributing to a low contact resistivity according to equation 3.4. What is more, the effective hole mass m^* is smaller for GeSn with higher Sn composition compared to Ge [72], which is also beneficial for a small contact resistivity as well as carrier injection.

A $Ge_{0.92}Sn_{0.08}$ layer is pseudomorphically grown on Ge virtual substrate. After nanowire patterning and digital etching, quasi-1D nanowire heterostructures may exhibit different strain distribution due to their unique boundary conditions compared to planar systems. According to finite element analysis based on the Matthews-Blakeslee equilibrium theory [224] and atomistic modeling [225], the anisotropic strain distribution of the in-plane strain σ_{xx} along the nanowire axial direction is displayed in Fig. 4.17 (b), the calculated strain is compressive (negative) in the GeSn overlayer and tensile (positive) in the Ge underlayer. Obviously, at the $Ge_{0.92}Sn_{0.08}$/Ge interface (z=0), in-plane σ_{xx} is the largest, +0.6 for the GeSn layer, and -0.6 for Ge layer, respectively, as it can be calculated as:

$$\sigma_{xx0} = \frac{a_{GeSn-} - a_{Ge}}{a_{GeSn+} + a_{Ge}} \tag{4.12}$$

Where a_{GeSn} and a_{Ge} are the relaxed lattice constants of GeSn and Ge, respectively.

The in-plane strain exponentially decays along the nanowire axis. Considering the nanowire is symmetrically circular, it follows:

$$\sigma_{xx} = \sigma_{yy} = \sigma_{xx0}\, e^{-\alpha|z|} \tag{4.13}$$

Where α is approximated to be 7/D (D is the nanowire diameter).

Fig. 4.17 (b) also compares the in-plane σ_{xx} as a function of z along the nanowire axial direction for GeSn/Ge nanowire heterostructures with diameters of 30 nm, 45 nm, and 65 nm. It is found that at the same z position, smaller nanowires exhibit smaller $|\sigma|$ or more relaxed lattice mismatch compared to larger nanowires, this also gives hints that hetero-epitaxy on

small nanowires can provide an effective option to relieve large lattice mismatch coherently. Similarly, the strain in the z-direction is given by

$$\sigma_{zz} = -\frac{C_{12}}{C_{11}}\sigma_{xx} \tag{4.14}$$

where C_{11} and C_{12} are the stiffness constants.

As is claimed, these strain values are calculated along the nanowire axis. In the radial direction, the strain can be estimated as $\propto \cos(\pi r/D)$, where r is the radial distance from the nanowire center. This means at the edge of small nanowires, the strain can be zero.

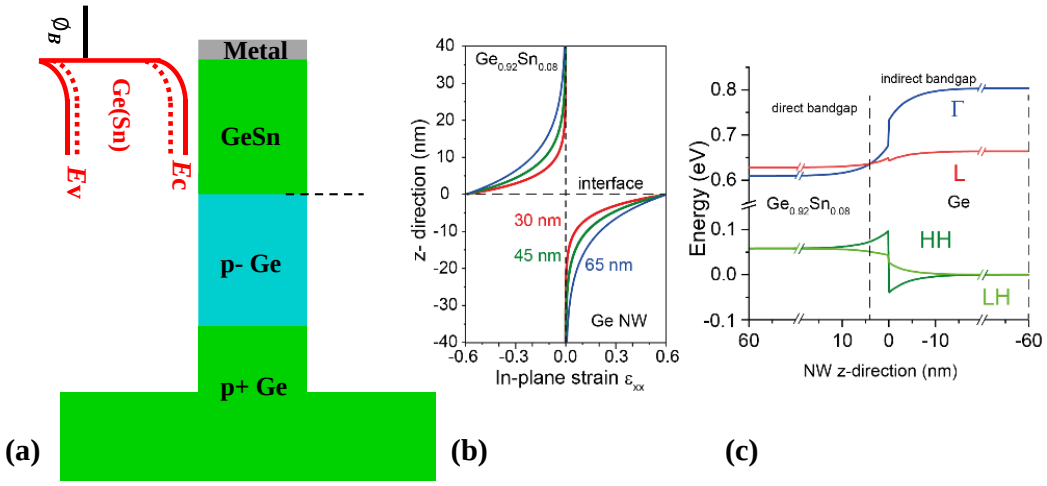

Fig. 4.17 (a) Schematic of GeSn/Ge nanowire with introducing a small bandgap GeSn material as the top layer to lower contact resistivity. (b) In-plane σ_{xx} as a function of z along the nanowire axial direction for GeSn/Ge nanowire heterostructures with diameters of 30 nm, 45 nm, and 65 nm. At the same z position, smaller nanowires exhibit smaller |σ| or more relaxed lattice mismatch compared to larger nanowires. (c) The $Ge_{0.92}Sn_{0.08}$/Ge band alignment along the axial direction with D = 30 nm, taking Sn content and strain effects into account. The band alignment is type I. At z=0, ΔE_C and ΔE_V exist at the GeSn/Ge interface, reproduced from [226].

The $Ge_{0.92}Sn_{0.08}$/Ge band alignment along the axial direction, which is also the carrier transportation direction, is shown in Fig. 4.17(c) with D = 30 nm, taking Sn content and strain effects into account. The electronic band structures of GeSn and Ge are carried out by the eight-band **k p** method [227] (Band structure calculation was conducted by Zoran Ikonic at University of Leeds). The band alignment between GeSn and Ge is the type I. At z=0, ΔE_C and ΔE_V exist at the GeSn/Ge interface. Since this work focuses on the holes for pMOSFETs, ΔE_V is paid great attention, which will affect carrier transport and the DIBL

effect addressed later. In addition, at approximately 5 nm away from the interface in GeSn overlayer, GeSn has a transition to a direct bandgap of $E_{g,\Gamma}$ = 0.551 eV, and $E_{g,L}$ = 0.570 eV since strain decays to a low level. This can further shrink the bandgap and the Schottky barrier height, contributing to a lowered contact resistivity and contact resistance.

GeSn/Ge Material characterization

The material stack of GeSn/Ge heterostructure is grown as shown in Fig. 3.2 (b). It starts with a 200 nm Ge layer with *in-situ* Boron doping on 200 mm Ge virtual substrate in the reduced pressure CVD, followed by 150 nm unintentionally doped Ge layer as the channel. The hetero-epitaxy ends with a 60 nm $Ge_{0.92}Sn_{0.08}$ layer. The cross-sectional TEM image in Fig. 4.18 (a) shows the 60 nm GeSn layer on a Ge virtual substrate. Fig. 4.18 (b-c) are high-resolution TEM images, demonstrating the high crystalline quality of the $Ge_{0.92}Sn_{0.08}$ layer and the defect-free interface between GeSn and Ge. A substitutional Sn content of ~8.3% is also confirmed by Rutherford backscattering spectrometry (RBS) measurement. The reciprocal space mapping (RSM) (Fig. 4.18 (d)) depicts that the peaks of GeSn and Ge lie along the same in-plane lattice vector, also confirming the GeSn layer is fully strained. The biaxial compressive strain value within the $Ge_{0.92}Sn_{0.08}$ layer is calculated to be 1.07% with respect to the relaxed sample and for Ge, it is 0.16% biaxially tensile strained.

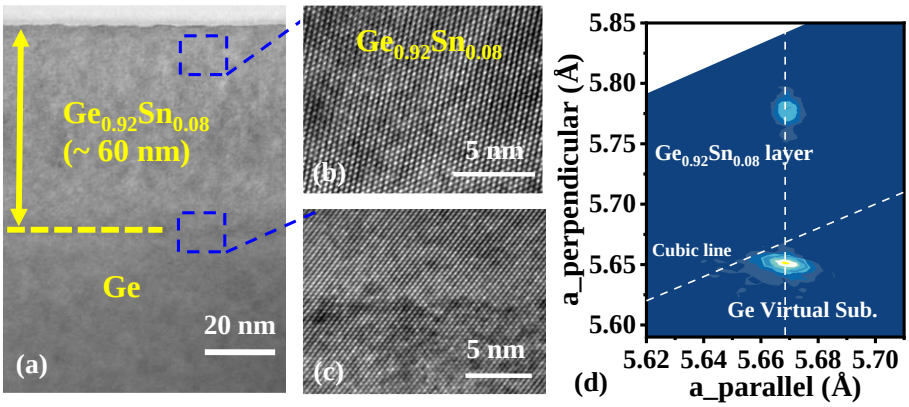

Fig. 4.18 (a) Cross-sectional TEM image of a 60 nm $Ge_{0.92}Sn_{0.08}$ layer on a Ge virtual substrate. (b) High-resolution TEM image of GeSn film indicating high crystalline quality and (c) the defect-free interface between GeSn and Ge. TEM measured by Jin Hee Bae, PGI-9, Forschungsentrum Juelich. (d) RSM for a GeSn layer on Ge: the peaks of $Ge_{0.92}Sn_{0.08}$ and Ge lie along the same in-plane lattice vector, indicating the GeSn layer is fully strained.

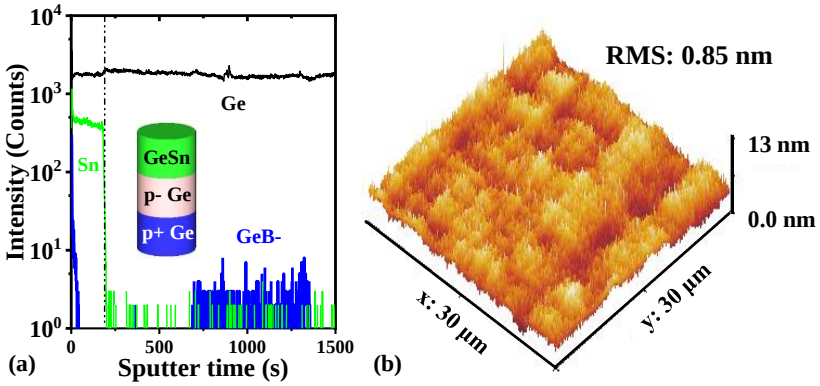

Fig. 4.19 (a) TOF-SIMS depth profiles of Ge, Sn and B atoms for a 60 nm $Ge_{0.92}Sn_{0.08}$ layer on Ge. It shows an abrupt interface and no apparent intermixing between GeSn and Ge layers. (b) AFM image showing the cross-hatched surface of the GeSn layer with the root mean square roughness of ~ 0.85 nm.

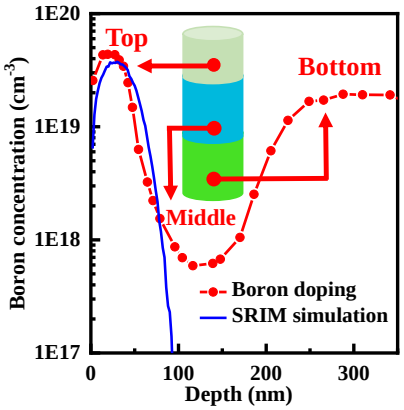

Fig. 4.20 The simulated and experimental Boron distribution with ion implantation in the GeSn layer. The peak activated doping concentration of ~ 5×10^{19} cm^{-3} can be obtained. The deviation for simulated and experimental profiles lies in dopants annealing in the experiment and broadening effects in the ECV measurement.

Time of flight secondary ion mass spectroscopy (TOF-SIMS) is applied to investigate the depth profiling for GeSn/Ge material stacks. In this end, a vertical profile of the elements can be recorded. Fig. 4.19 (a) depicts TOF-SIMS depth profiles of Ge, Sn, and B atoms for a 60 nm $Ge_{0.92}Sn_{0.08}$ layer on Ge. It shows an abrupt interface and no apparent intermixing between GeSn and Ge layers. Because GeSn growth is performed at a low temperature to avoid Sn segregation. Boron-doped Ge bottom layer is also confirmed (Blue curve). AFM image in Fig. 4.19 (b) shows the cross-hatched surface of the GeSn layer on Ge with the root mean square roughness of ~ 0.85 nm. This pattern is typical for regular misfit dislocations at the underlying Ge virtual substrate on Si [228]. Digital etching can be used to further smoothen the GeSn surface.

In the top GeSn layer, it is grown without *in-situ* doping to keep the good material quality. Therefore, Boron ion implantation is implemented. Firstly, Boron distribution in the GeSn layer is simulated according to the Stopping and Range of Ions in Matter (SRIM) in Fig. 4.20 (blue line). It is performed with a dose of 2 $\times 10^{14}$ cm^{-2} and an energy of 10 keV. The parameters are chosen to form an appropriate position of peak Boron concentration. Combining the thickness of sputtered Ni, it is aimed at forming a good NiGeSn contact with low contact resistivity. Afterwards, low-temperature annealing at 400 ℃ is adopted to guarantee the material integrity and maximum activated doping concentration. Fig. 4.20 shows the ECV measurement of active Boron doping concentration. The peak activated doping concentration of ~ 5×10^{19} cm^{-3} can be achieved in the GeSn layer. Both simulated and experimental profiles almost overlap, the deviation potentially lies in dopants annealing in the experiment and the ECV measurement errors.

4.4.1. Top contact resistance reduction by NiGeSn metallization

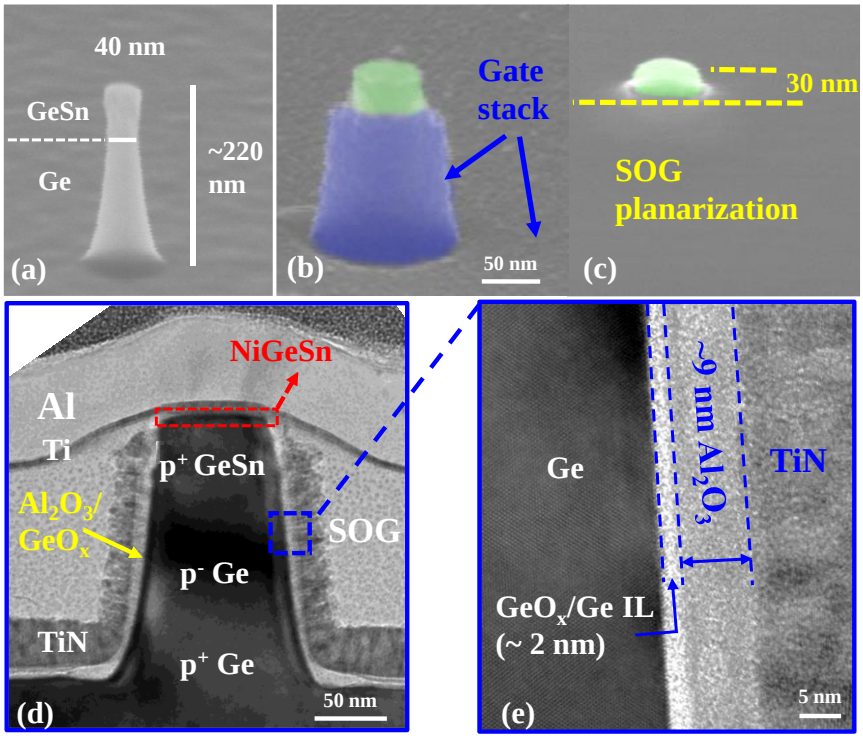

Fig. 4.21 (a) SEM image of a vertical GeSn/Ge nanowire with a diameter of 40 nm and a height of 220 nm after nanowire patterning and digital etching. (b) False-color SEM image of a top gate stack recess and (c) the second planarization step. The top 30 nm is exposed for NiGeSn metallization. (d) Cross-sectional TEM image of the fabricated device, featuring NiGeSn metallization, TiN/Al_2O_3/GeO_x gate stack, and 3D stack layers. (e) High-resolution TEM image of good quality gate stack on Ge channel with a 2 nm GeO_x IL.

Vertical $Ge_{0.92}Sn_{0.08}$/Ge GAA nanowire pMOSFETs are fabricated by the process flow introduced in session 4.1. Fig. 4.21 (a) shows the SEM image of a single vertical GeSn/Ge nanowire with a diameter of 40 nm and a height of 220 nm. The dielectric stack used here is 9 nm Al_2O_3/~2 nm GeO_x with the post-oxidation process by the rapid thermal oxidation (EOT = 5 nm). Figs. 4.21 (b-c) correspond to the SEM images of the top gate stack recess and the second planarization processes. In the top contact formation, to investigate the influence of Ni sputtering, two control experiments with and without Ni are compared in terms of key electrical FOMs. The devices end with contact pad formation, as shown in the TEM image (Fig. 4.21 (d)). It features NiGeSn metallization, gate stack, and 3D stack layers. The high-resolution TEM image of a good quality TiN/Al_2O_3/GeO_x gate stack is depicted in Fig. 4.21 (e). It is emphasized that each process step keeps a low thermal budget of <400 ℃ to avoid Sn segregation.

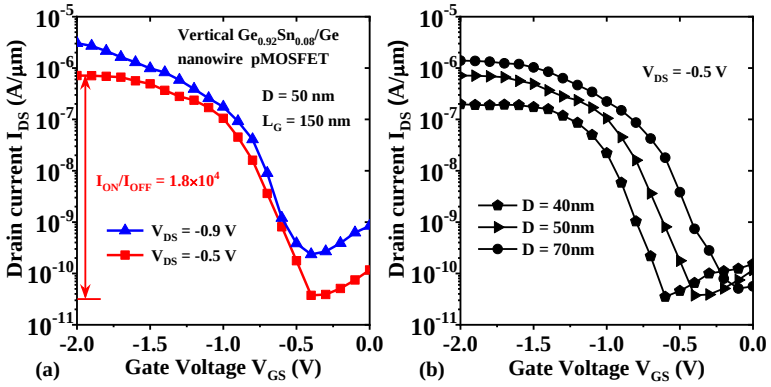

Fig. 4.22 (a) I_{DS}-V_{GS} transfer characteristics of the fabricated single vertical $Ge_{0.92}Sn_{0.08}$/Ge GAA nanowire pMOSFET with a diameter of 50 nm at V_{DS} of -0.1V and -0.5V. The measurement is in the TCS configuration. An I_{ON}/I_{OFF} ratio of ~1.8×10^4 is obtained at V_{DS} = -0.5 V. (b) The transfer characteristics of GeSn/Ge nanowire pMOSFETs with various diameters at V_{DS} = -0.5 V. The devices exhibit higher on-state currents with increasing nanowire diameters.

The I_{DS}-V_{GS} transfer characteristics of the fabricated single vertical $Ge_{0.92}Sn_{0.08}$/Ge GAA nanowire pMOSFET with a diameter of 50 nm are shown in Fig. 4.22 (a) with an I_{ON}/I_{OFF} ratio of ~1.8×10^4 at V_{DS} = -0.5 V. The measurement is in the TCS configuration. The use of a larger bandgap Ge at the drain side instead of a smaller bandgap GeSn can suppress GIDL, leading to small off-currents. The transfer characteristics of GeSn/Ge nanowire pMOSFETs with various diameters at V_{DS} = -0.5 V are also compared in Fig. 4.22 (b). The devices exhibit higher on-state currents with increasing nanowire diameters. This electrical behavior is in good qualitative agreement with Ge nanowire devices shown in session 4.3. It is already

explained that the total resistance R_{tot} is determined primarily by the top source resistance R_S, a larger nanowire device contributes to a smaller R_S, therefore exhibiting smaller R_{tot} and a higher I_{ON}. This R_{tot} trend with nanowire diameters is plotted in Fig. 4.25 (blue curve). R_{tot} decreases with increasing nanowire diameters. R_{tot} achieves 1.9 $\times 10^3$ kΩ·μm at a diameter of 70 nm, the value is so large that optimization on the top contact should be conducted in the following work. Meanwhile, the off-state currents I_{OFF} in these transistors barely increase with the diameters, due to the same channel-to-drain structures for all devices.

As is presented in Ge nanowire pMOSFETs in session 4.3, *SS* decreases with nanowire diameters, which corresponds to improved gate electrostatic integrity of GAA nanowires. However, GeSn/Ge devices exhibit no apparent SS dependence on diameters as shown in the left axis in Fig. 4.23 (a). *SS* is extracted at V_{DS} of -0.5 V. It can be explained by Equation 4.6, the large top source contact resistance resulting from a small contact area deteriorates *SS* a lot. Therefore, the interplay between diameter-related electrostatics and top source resistance results in similar SS in this experiment. The I_{ON}/I_{OFF} ratio is provided in Fig. 4.23 (a) (right-axis). Transistors with diameters of 70 nm have a decent I_{ON}/I_{OFF} ratio of ~4×10^4 at V_{DS} = -0.5V. The improved I_{ON}/I_{OFF} ratio with the nanowire diameters can be attributed to the reduction of the top source resistance. $G_{m,ext}$ as a function of V_{GS} is shown in Fig. 4.23 (b) at V_{DS} of -0.5V. With considerable R_S and R_{tot} in the GeSn/Ge nanowire pMOSFETs, devices with 40, 50 and 70 nm diameters exhibit low $G_{m,ext}$. This also points out the necessity of reducing R_S and R_{tot}. The peak $G_{m,ext}$ increases with increasing nanowire diameters, showing a similar trend as the aforementioned Ge nanowire pMOSFETs.

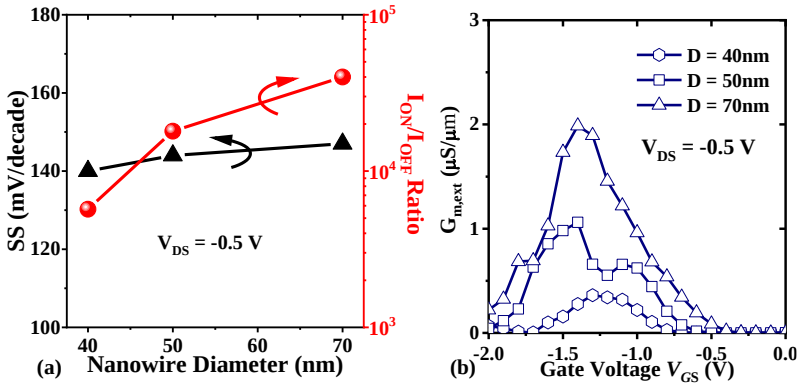

Fig. 4.23 (a) Comparison of SS (left-axis) and I_{ON}/I_{OFF} ratio (right-axis) for vertical $Ge_{0.92}Sn_{0.08}$/Ge GAA nanowire pMOSFETs with different diameters at V_{DS} = -0.5V. GeSn/Ge devices exhibit no apparent SS dependence on diameters. The improved I_{ON}/I_{OFF} ratio for larger diameters devices can be attributed to the reduction of the top source resistance. (b) $G_{m,ext}$ as a function of V_{GS}. The devices with 40, 50 and 70 nm diameters exhibit low $G_{m,ext}$ due to large R_S and R_{tot}.

In order to reduce the top contact resistance and improve the on-state performance of $Ge_{0.92}Sn_{0.08}$/Ge GAA nanowire pMOSFETs, here the optimization of NiGeSn metallization for the top source is applied. 6 nm thick Ni layer is sputtered on the top nanowire and then annealed at 325 ℃ for 15s in forming gas atmosphere to suppress Sn segregation and obtain a low contact resistivity. The other process steps keep the same. Fig. 4.24 shows the transfer and output characteristics for GeSn/Ge device with a diameter of 32 nm. With NiGeSn metallization and a small nanowire diameter, good subthreshold properties with *SS* of 72 mV/decade and a high I_{ON}/I_{OFF} ratio of 3×10^6 at V_{DS} = -0.1V are obtained (Fig. 4.24(a)). The output characteristics in Fig. 4.24 (b) shows a good saturation property at V_{GS} from 0 to -1V.

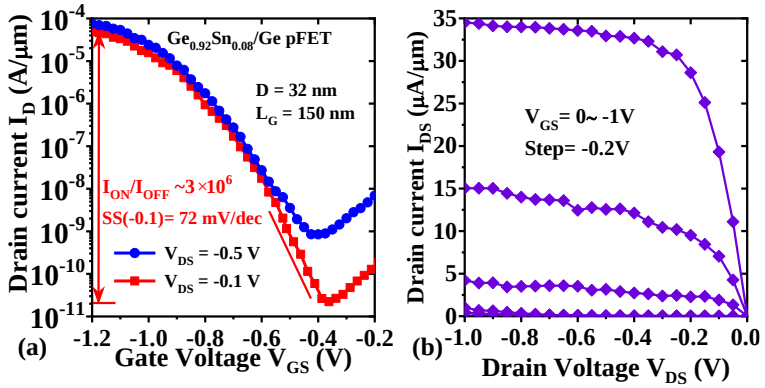

Fig. 4.24 Transfer (a) and output (b) characteristics for GeSn/Ge device with a diameter of 32 nm. With NiGeSn metallization and a small nanowire diameter of 32 nm, good subthreshold properties with a *SS* of 72 mV/decade and a high I_{ON}/I_{OFF} ratio of 3×10^6 are obtained.

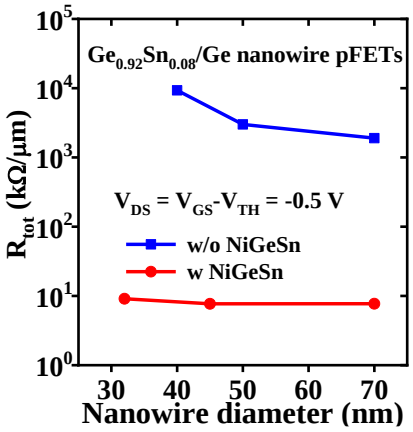

Fig. 4.25 Extracted R_{tot} trend with various diameters for GeSn/Ge nanowire pFETs with and without NiGeSn metallization. As NiGeSn metallization is adopted, R_{tot} drops dramatically and keeps roughly constant at ~8 kΩ·μm no matter what the nanowire diameter is.

From the analysis in Fig. 4.24, apparent electrical advantages for GeSn/Ge devices with NiGeSn metallization have been gained in terms of *SS*, I_{ON}, and I_{ON}/I_{OFF} ratio compared with those without NiGeSn metallization. Since the introduction of NiGeSn greatly decreases the top contact resistance, nanowire diameters have then a weakened influence on the R_S and R_{tot}. Therefore, diameter-related electrostatic control is thus the major factor that needs to be considered. This is confirmed by the extracted R_{tot} trend with various diameters in Fig. 4.25. For the pFET with a 40 nm diameter without NiGeSn, the total resistance is incredibly high, 9.3 $\times 10^3$ kΩ·μm, which greatly hampers the on-state performance. As NiGeSn metallization is adopted, R_{tot} drops dramatically and keeps roughly constant at ~8 kΩ·μm no matter what the nanowire diameter is. This means that, for the devices with NiGeSn metallization, the nanowire diameter is not a limiting factor of R_S and R_{tot}. Nevertheless, further R_{tot} reduction should be conducted for performance improvement.

4.4.2. Performance improvement by GeSn

In this part, with the well-developed NiGeSn metal contact as shown in the previous session, material options of GeSn versus Ge have been applied for the performance comparison, the effect of GeSn as the source layer will be highlighted compared to the Ge control devices. The measurement is in the TCS configuration. The vertical GeSn/Ge nanowire pMOSFET with a diameter of 65 nm achieves *SS* of 84 mV/decade and a high I_{ON}/I_{OFF} ratio of ~8.4×10^5 at V_{DS} = -0.1V thanks to GAA nanowire geometry and good surface passivation (Fig. 4.26 (a)). For the Ge control pMOSFET with the same nanowire diameter in Fig. 4.26 (b), a low *SS* of 68 mV/decade is extracted. The *SS* difference will be addressed in Fig. 4.28 (a). The performance improvement by utilizing GeSn as a source than Ge is demonstrated in the I_D-V_{DS} output characteristics comparison (Fig. 4.26(c)). At V_{GS}-V_{TH} = -0.5V and V_{DS} = -1V, ~32% I_{ON} enhancement is observed for GeSn/Ge device compared to Ge one. This improvement is attributed to the smaller total resistance R_{tot} and higher transconductance $G_{m,ext}$ in GeSn/Ge devices as confirmed in Fig. 4.27.

Fig. 4.27 (a) shows R_{tot} versus nanowire diameters for GeSn/Ge and Ge nanowire pMOSFETs. GeSn/Ge nanowire pMOSFETs demonstrate smaller R_{tot} than Ge devices with various nanowire diameters. Thanks to Fermi level pinning close to E_V in Ge(Sn) and a small bandgap in GeSn, the effective Schottky barrier height Φ_B of $NiGe_{0.92}Sn_{0.08}/Ge_{0.92}Sn_{0.08}$ is smaller than that of NiGe/Ge (inset of Fig. 4.27 (a)), leading to a smaller contact resistivity, R_S and thus R_{tot}. On the contrary, $G_{m,ext}$, and G_{max} have opposite behaviors. Fig. 4.27 (b) plots G_{max} as a function of nanowire diameters for GeSn/Ge and Ge pMOSFETs. Both devices exhibit higher

G_{max} with increasing nanowire diameters and G_{max} for GeSn/Ge devices is larger than that for Ge devices.

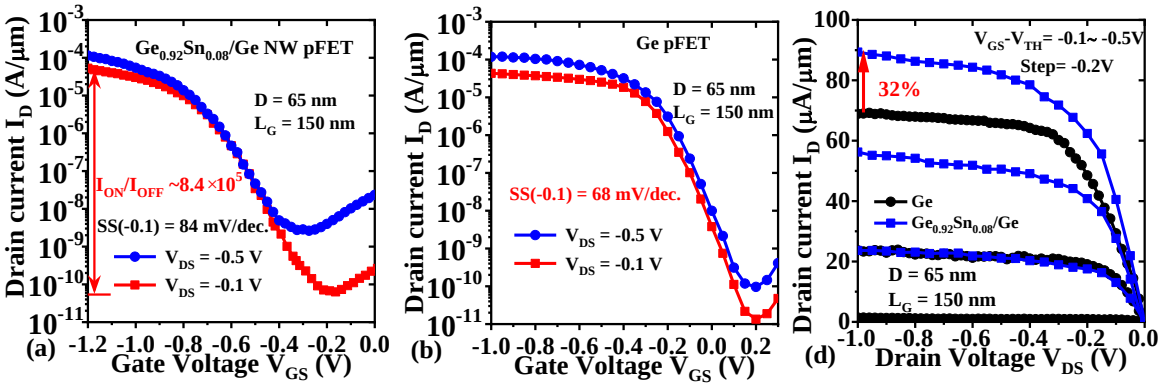

Fig. 4.26 I_D-V_{GS} transfer characteristics of a $Ge_{0.92}Sn_{0.08}$/Ge GAA nanowire pMOSFET with a diameter of 65 nm. Low *SS* of 84 mV/dec and a high I_{ON}/I_{OFF} ratio of ~8.4×10^5 at V_{DS} = -0.1V are obtained. (b) I_D-V_{GS} curves of a 65 nm diameter Ge nanowire pFET with low *SS* of 68 mV/decade. (c) I_D-V_{DS} comparison between $Ge_{0.92}Sn_{0.08}$/Ge and Ge nanowire pFETs. At V_{GS}-V_{TH} = -0.5V, ~32% I_{ON} improvement is observed for GeSn/Ge device compared with Ge one.

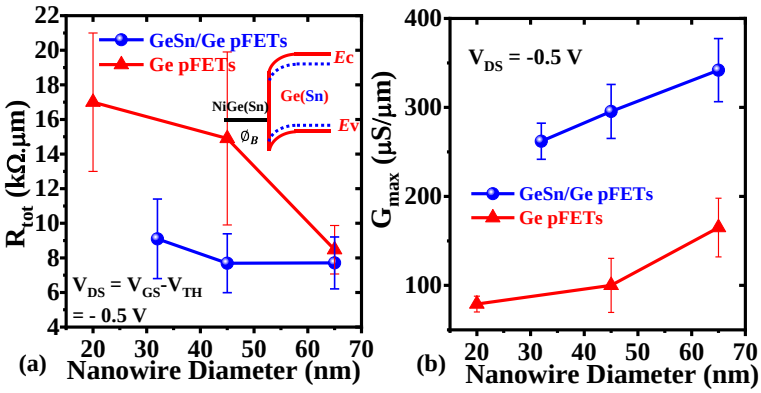

Fig. 4.27 (a) R_{tot} versus nanowire diameters for GeSn/Ge and Ge nanowire pFETs. R_{tot} for both devices shows a decreasing trend with increasing nanowire diameters. GeSn/Ge pFETs demonstrate smaller R_{tot} than Ge devices with various nanowire diameters. Inset: Φ_B of $NiGe_{0.92}Sn_{0.08}/Ge_{0.92}Sn_{0.08}$ is smaller than that of NiGe/Ge, leading to a smaller contact resistivity. (b) G_{max} as a function of nanowire diameters for GeSn/Ge and Ge pFETs. Devices exhibit higher G_{max} with increasing nanowire diameters and G_{max} for GeSn/Ge devices is larger than that for Ge devices.

Further analysis of the impact of electrical FOMs e.g. *SS*, DIBL on nanowire diameters for GeSn/Ge, and Ge nanowire pMOSFETs are carried out to show the advantage of GeSn source over Ge. Fig. 4.28 (a) depicts *SS* scaling metrics versus nanowire diameters. Generally,

GeSn/Ge pMOSFETs exhibit larger *SS* than the Ge devices and for GeSn/Ge devices, the *SS* at V_{DS} of -0.1V and -0.5V shows more spreading compared to Ge devices. This can be attributed to higher D_{it} resulting from O_2 plasma post-oxidation for GeSn/Ge pMOSFETs instead of thermal oxidation for Ge pMOSFETs. As is expressed in Equation 4.10, higher D_{it} leads to larger interface state capacitance and thereby larger *SS*. What is more, as expected, *SS* decreases with nanowire diameters for GeSn/Ge pMOSFETs due to improved gate control. V_{TH} as a function of various nanowire diameters is shown in Fig. 4.28 (b). V_{TH} decreases as nanowire diameters shrink for both devices. Part of V_{GS} drop on R_S should be taken into account to explain V_{TH} scaling rules. In addition, a negative V_{TH} shift in GeSn/Ge nanowire pFETs is seen compared with Ge pFETs. It's speculated that larger potential screening resulting from higher D_{it} at the interface can lead to this phenomenon for GeSn/Ge pMOSFETs and charge trapping effect within the dielectric can also potentially affect. Sufficient surface passivation and good-quality high-κ dielectric have to be developed for GeSn/Ge devices.

One interesting phenomenon for GeSn/Ge pMOSFETs is DIBL behavior. In the analysis of the DIBL scaling trend in Ge pMOSFETs (red curve in Fig. 4.28 (c)), DIBL increases with increasing nanowire diameters, whereas DIBL in GeSn/Ge pMOSFETs stays almost constant. This behavior may appear not necessarily correct at first sight. Using the capacitor representation based on a top-of-the-barrier model, DIBL can be written as:

$$DIBL = \frac{C_D}{C_{ox} + C_D + C_{it}} \tag{4.15}$$

This indicates that DIBL is inversely proportional to C_{it}, if C_{it} is sufficiently large due to a high D_{it}, DIBL can be lowered. As a consequence, Ge devices exhibit an increase of DIBL with diameters thanks to a small D_{it}, while in the case of GeSn/Ge devices, C_{it} is expected to be large enough because of low-temperature O_2 plasma passivation and consequently a smaller DIBL is obtained in Fig. 4.28 (c) (blue curve). Nevertheless, this simple model can explain the small DIBL in the GeSn/Ge devices, it does not give an accurate description of the approximately constant DIBL trend. Then it is suggested that a valence band offset ΔE_v at the hetero-interface between $Ge_{0.92}Sn_{0.08}$ and Ge should be considered (inset of Fig. 4.28 (c)). As is shown in Fig. 4.17 (c), the strain at the GeSn/Ge hetero-interface has a different impact on the valence bands: light- and heavy-hole bands (LH and HH). While a large valence band offset exhibits at the HH, the LH shows only a very small valence offset. Therefore, a dipole layer accumulates at the hetero-interface in the HH, lowering the impact of the applied drain bias, since it is screened by the large carrier density within this dipole layer. This can

potentially reduce the drain current. However, the potential barrier is negligible for the light holes at LH. In short, the heavy holes result in a rather stationary charge that diminishes DIBL while the light holes are beneficical for the drain current [226]. As a result, the particular GeSn/Ge heterostructure along with an appropriate strain field, yields a major scaling benefit compared to Ge homojunction devices.

In order to scrutinize the assumption regarding the impact of the GeSn/Ge heterostructure on the suppression of DIBL, self-consistent device simulations based on the non-equilibrium Green's function formalism (NEGF) are performed (Simulation was done by Prof. Joachim Knoch at RWTH Aachen University). The heterostructure offsets and the impact of strain on the LH and HH are extracted from the calculations in Fig. 4.17. Fig. 4.28 (d) displays DIBL values extracted from the simulation at V_{GS} = 0V. It is noted that to decrease the computational burden, a shorter device (L_g= 20 nm) is considered here in comparison with the experimental devices. From the simulation, the DIBL is significantly larger than that in the experiment due to short channel effects, however, the scaling trend of DIBL with nanowire diameters stays approximately constant, which is similar to the experimental values in this part. This well-reproduced behavior further confirms the advantage of GeSn/Ge heterostructures.

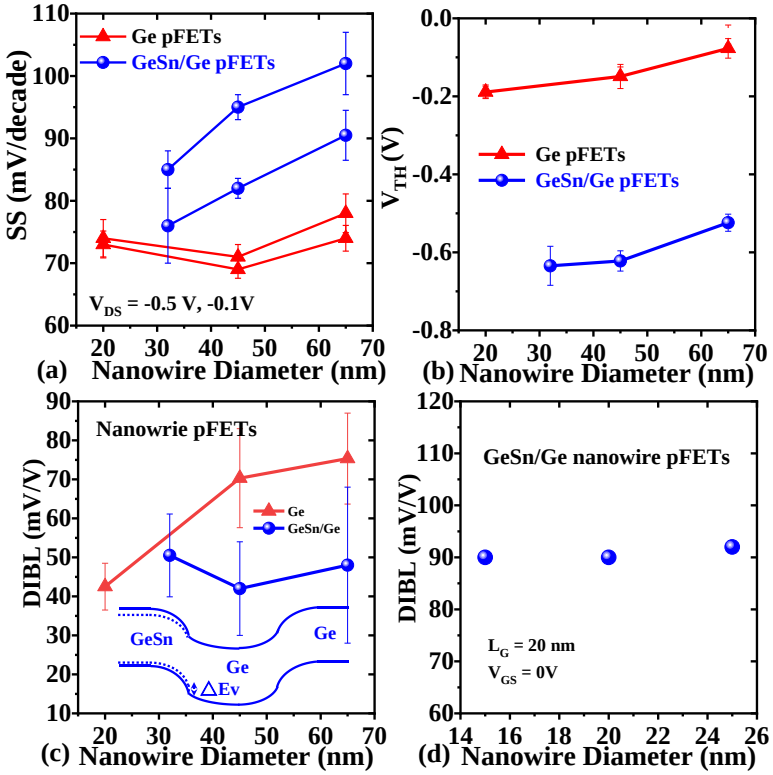

Fig. 4.28 (a) *SS* scaling metrics versus nanowire diameters for GeSn/Ge and Ge pFETs. GeSn/Ge pFETs exhibit larger *SS* than the Ge devices. (b) V_{TH} as a function of various

nanowire diameters. V_{TH} decreases as nanowire diameters shrink for both devices. A negative V_{TH} shift in GeSn/Ge nanowire pFETs is seen compared with Ge pFETs. (c) DIBL scaling trend with diameters. DIBL in GeSn/Ge pMOSFETs stays almost constant and exhibits lower values compared to Ge devices. Inset: ΔE_v at the hetero-interface between $Ge_{0.92}Sn_{0.08}$ and Ge is beneficial to suppress the DIBL. (d) Simulated DIBL values at V_{GS} = 0V and short L_g = 20 nm [226]. The scaling trend of DIBL is similar to the experimental values.

4.4.3. EOT scaling

EOT in the previous nanowire pMOSFETs is ~ 5 nm. In this session, the influence of EOT scaling, along with nanowire diameter scaling on the electrical characteristics is compared for GeSn/Ge heterostructure and Ge homostructure nanowire pMOSFETs.

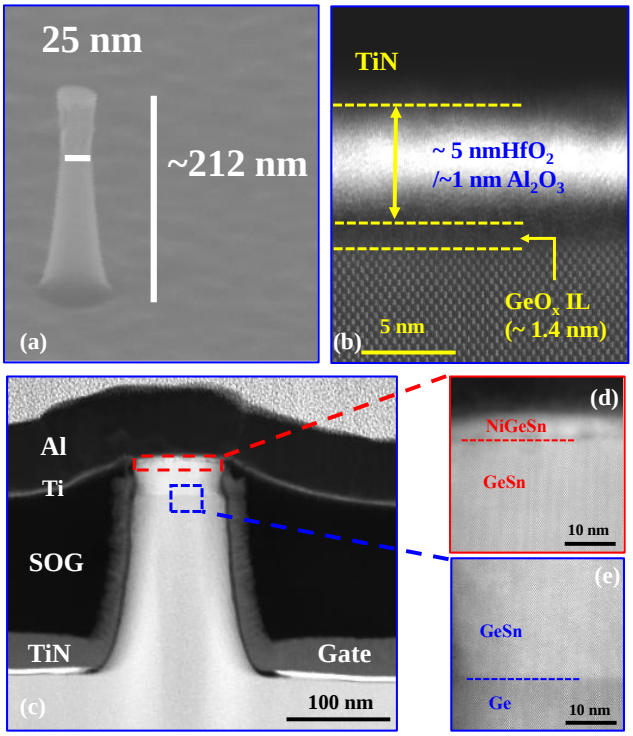

Fig. 4.29 (a) Tilted SEM image of a vertical GeSn/Ge nanowire with D = 25 nm, exhibiting smooth sidewalls and a height of ~212 nm. (b) TEM image of gate stack consisting of ~ 5 nm HfO_2 and ~1.4 nm GeO_x (EOT = ~ 2 nm). (c) TEM image of the fabricated GeSn/Ge nanowire with 3D stacked layers. (d) High-resolution TEM image emphasizing the interface between $NiGe_{0.92}Sn_{0.08}$ and $Ge_{0.92}Sn_{0.08}$. (e) The high crystalline quality of GeSn and a defect-free interface between GeSn and Ge. FIB preparation and TEM measurement by Jin Hee Bae, PGI-9, Forschungsentrum Juelich.

The process flow for vertical GeSn/Ge nanowire pMOSFETs is similar to session 4.4.2 except for the dielectrics chosen for a smaller EOT. Fig. 4.29 (a) depicts a tilted SEM image of a

vertical GeSn/Ge nanowire with D = 25 nm, exhibiting smooth sidewalls and a height of ~212 nm. The dielectric combination of ~ 5 nm HfO_2 and ~1 nm Al_2O_3, with ~1.4 nm GeO_x interfacial layer forms EOT of ~ 2 nm considering ε_{GeOx} and ε_{HfO2} are 6 and 18, respectively (Fig. 4.29 (b)). Note that GeO_x is generated by post-oxidation with O_2 plasma. The fabricated GeSn/Ge nanowire device is shown by the TEM image with 3D stacked layers in Fig. 4. 29 (c). Fig. 4.29 (d) emphasizes the interface between $NiGe_{0.92}Sn_{0.08}$ and $Ge_{0.92}Sn_{0.08}$, and (e) shows the high crystalline quality of GeSn and a defect-free interface between GeSn and Ge. Fig. 4.30 (a) presents I_D-V_{GS} transfer characteristics of a single vertical $Ge_{0.92}Sn_{0.08}$/Ge GAA nanowire pMOSFET with a diameter of 25 nm. Great gate electrostatics can be reflected in the key FOMs: low *SS* of 67 mV/decade and an I_{ON}/I_{OFF} ratio of ~10^6 at V_{DS} = -0.1V are obtained. I_D-V_{DS} output curves of the device are plotted in Fig. 4.30 (b), showing good current saturation. A drain current of ~108 µA/µm is achieved at V_{GS} - V_{TH} =-0.6V. The drain current fluctuation is attributed to the discrete charge trapping by the dielectric or interface defects in small nanowire transistors [208].

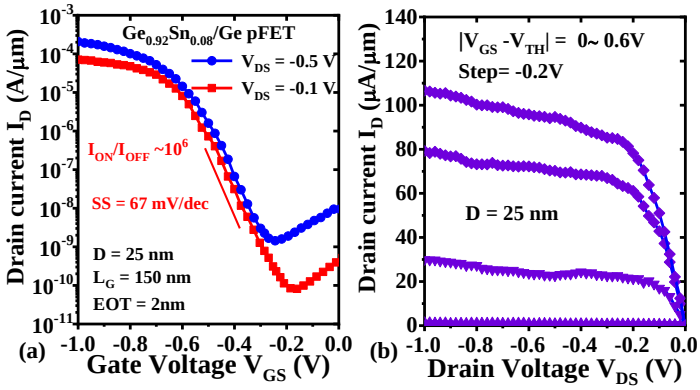

Fig. 4.30 (a) I_D-V_{GS} transfer characteristics of a single vertical $Ge_{0.92}Sn_{0.08}$/Ge GAA nanowire pMOSFET with a diameter of 25 nm and EOT of 2 nm. Low *SS* of 67 mV/decade and an I_{ON}/I_{OFF} ratio of ~10^6 at V_{DS} = -0.1V are obtained. (b) I_D-V_{DS} output curves, showing good current saturation. A drain current of ~108 µA/µm is achieved at V_{GS} - V_{TH} =-0.6V.

Fig. 4.31 (a) compares the I_D-V_{GS} curves for 65 nm diameter GeSn/Ge nanowire devices with various EOT. Note that the results with EOT =5 nm are taken from session 4.4.2. Obviously, a significant I_{ON} improvement is reached by scaling EOT from 5 nm down to 2 nm, which can be simply explained by $I_{ON} \propto C_{ox}(V_{GS} - V_{TH})^2$. Note that DIBL in the device with EOT = 2nm exhibit larger than that with EOT = 5nm, probably due to charge trapping in the dielectric. Nevertheless, the *SS* stays similar for both devices, ~89 mV/decade, highlighting good gate controllability. As expected, devices with smaller EOT exhibit a positive V_{TH} shift through the expression:

$$V_{TH} = \frac{-|Q_D| - Q_s}{C_{ox}} + \emptyset_{ms} - 2\emptyset_{fn} \tag{4.16}$$

Where Q_D are the charges in the depletion region, Q_s is the equivalent oxide charge. $\emptyset_{ms}$ is the metal-Ge work function difference and $\emptyset_{fn}$ is the difference between E_{Fi} and E_F.

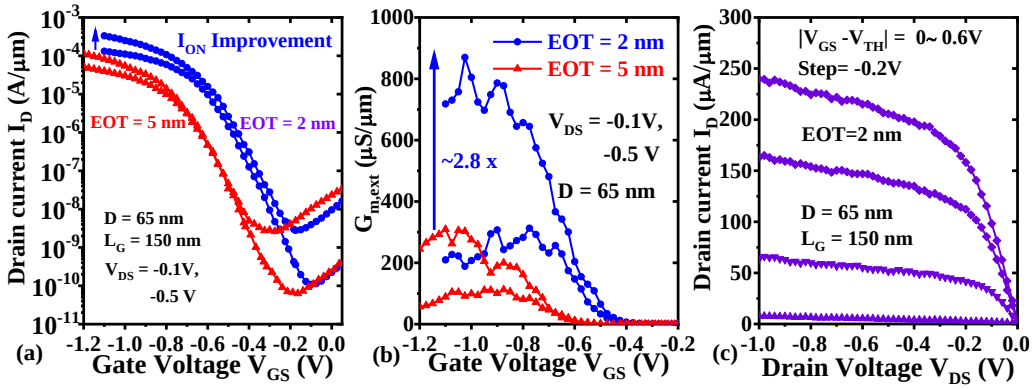

Fig. 4.31 (a) I_D-V_{GS} curves for 65 nm diameter GeSn/Ge nanowire devices with various EOT. A significant I_{ON} improvement is reached by scaling EOT from 5 nm down to 2 nm. (b) $G_{m,ext}$ characteristics for devices with EOT of 2 and 5 nm. The device with EOT = 2 nm yields the peak G_{max} of ~870 μS/μm at V_{DS} = -0.5V, which is ~2.8 times larger compared to G_{max} (~310 μS/μm) for the device with EOT = 5 nm. (c) I_D-V_{DS} output curves with a high drain current of ~245 μA/μm at V_{GS} - V_{TH} = -0.6V and V_{DS} = -1V.

The performance enhancement by EOT scaling is also embodied in the $G_{m,ext}$ characteristics (Fig. 4.31 (b)). The device with EOT = 2 nm yields the peak G_{max} of ~870 μS/μm at V_{DS} = -0.5V, which is ~2.8 times larger compared to G_{max} (~310 μS/μm) for the device with EOT = 5 nm. A high drain current of ~245 μA/μm is achieved at V_{GS} - V_{TH} = -0.6V and V_{DS} = -1V in the output curves (Fig. 4.31 (c)).

Next, the dependence of the key electrical FOMs on the EOT scaling and nanowire diameter scaling is discussed. Expectedly, *SS* for devices with EOT of 2 and 5 nm decreases with shrinking nanowire diameters from 65 nm to 25 nm. Moreover, the devices with smaller EOT have better *SS*, which is due to stronger electrostatic control (cf. Fig. 4.32 (a)). With the improved process and EOT scaling, R_{tot} in this session is not strongly dependent on nanowire diameters and remains constant at approximately 3.8 kΩ·μm (Fig. 4.32 (b)). Moreover, R_{tot} falls appreciably compared to Ge and GeSn/Ge nanowire pMOSFETs with EOT = 5nm shown before. The peak G_{max} as a function of nanowire diameters measured at V_{DS} = -0.5V is depicted in Fig. 4.32 (c). The devices with EOT = 2 nm exhibit larger G_{max} in comparison

with those GeSn/Ge and Ge nanowire pMOSFETs with EOT = 5 nm and all of these devices show increasing G_{max} with nanowire diameters.

Until now, the effect of EOT scaling on electrical performance is discussed in detail. However, the EOT of 2 nm in this work is still far from the state-of-the-art target of approximately sub-0.5 nm. Further EOT scaling should be developed considering reasonable D_{it} and reliability issues. What is more, the etching selectivity between high-κ dielectric and TiN metal during the top gate stack recess process is critical for vertical nanowire transistors. Aggressive EOT scaling requires the coordination of gate stack engineering and other process correlation during device fabrication.

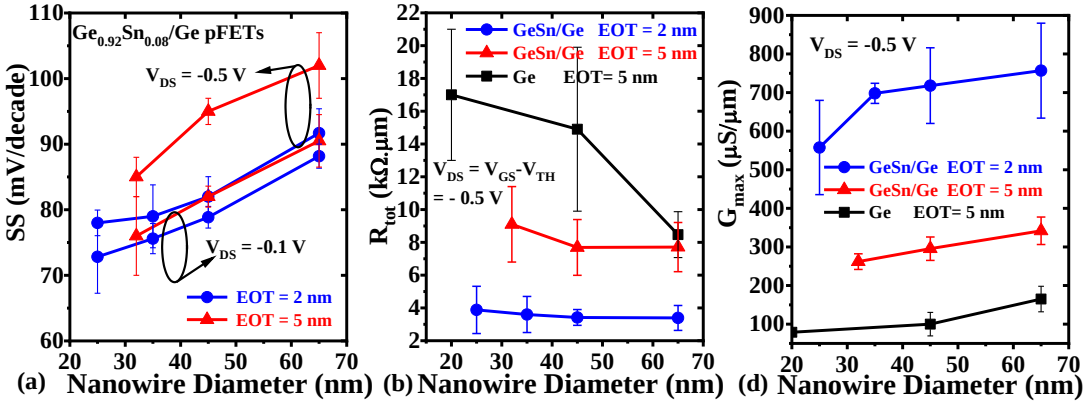

Fig. 4.32 (a) *SS* with diameter scaling from 65 nm to 25 nm. The devices with 2 nm EOT have better *SS*. (b) Dependence of R_{tot} on nanowire diameters for GeSn/Ge and Ge pFETs. R_{tot} for GeSn/Ge pFETs with EOT = 2nm remains constant at approximately 3.8 kΩ·μm. (c) Peak G_{max} with nanowire diameters measured at V_{DS} = -0.5V. The devices with EOT = 2 nm exhibit larger G_{max} in comparison with those GeSn/Ge and Ge nanowire pFETs with EOT = 5 nm.

Benchmark

Fig. 4.33(a) benchmarks *SS* with various Sn content among GeSn-based planar, Fin, and horizontal/vertical nanowire pMOSFETs. By utilizing appropriate surface passivation with the post-oxidation process and GAA nanowire geometry, the devices in this work achieve the low *SS* of 67 mV/decade for $Ge_{0.92}Sn_{0.08}$/Ge nanowire pMOSFETs. To the best knowledge, this is the first demonstration of vertical GeSn-based nanowire pMOSFETs by a top-down approach and this value is lowest in any GeSn-based nanowire pMOSFETs (cf. Fig. 4.33 (b)). The transport and electrostatics properties among GeSn-based pMOSFETs recently published in the literature are also benchmarked in Fig. 4.33 (c). The devices demonstrate the highest G_{max} of ~870 μS/μm and the best quality factor $Q = G_{max}/SS_{sat}$ of ~9.1 for any GeSn-based

pMOSFETs. In short, the good performance for vertical GeSn/Ge nanowire pMOSFETs is attributed to the superior gate electrostatic integrity and process optimization on surface passivation, contact metallization etc. These results highlight the potential of GeSn-based nanowire transistors for low power applications.

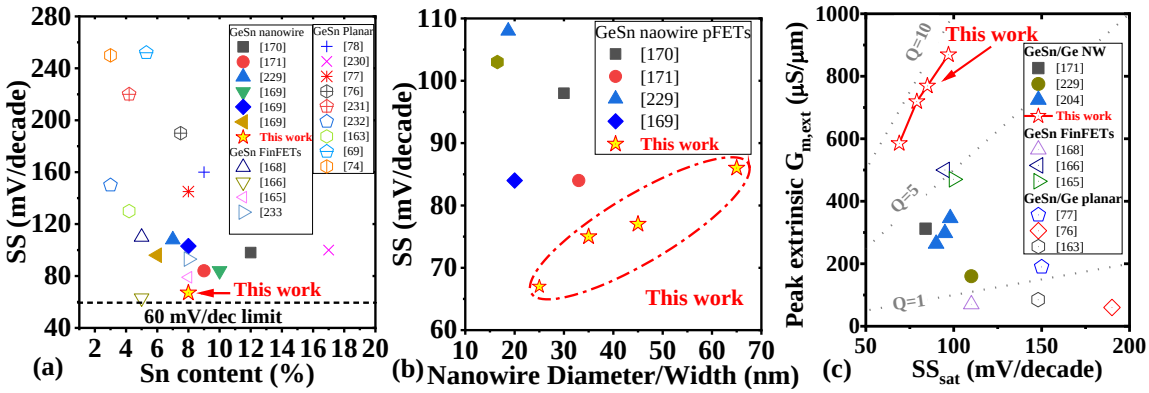

Fig. 4.33 (a) Benchmark of *SS* with various Sn content among GeSn-based planar, Fin, and horizontal/vertical nanowire pMOSFETs. The devices achieve a low *SS* of 67 mV/decade for $Ge_{0.92}Sn_{0.08}$/Ge nanowire pMOSFETs. (b) Benchmark of *SS* with nanowire diameters/widths among GeSn-based nanowire pMOSFETs. (c) Benchmark of $Q = G_{max}/SS_{sat}$ at V_{DS} = -0.5V. The devices shown in this work demonstrate the highest G_{max} of ~870 μS/μm and the best quality factor *Q* of ~9.1 for any GeSn-based pFETs.

4.5. Conclusion

In this chapter, a detailed process flow for vertical GAA nanowire MOSFETs is introduced and applied to Ge(Sn)-based nanowire pMOSFETs. In the undoped Ge nanowire pMOSFET, it is emphasized that an appropriate doping profile for Ge nanowire pMOSFETs is required to form excellent Ohmic contacts and the reasonable gate alignment towards source/drain. Vertical Ge nanowire pMOSFETs based on Ge p^+-p^--p^+ doping are thereby demonstrated. A systematical study of the impact of nanowire diameter scaling on key electrical FOMs are conducted. The transistors follow the classical diameter scaling properties. The devices with 65 nm diameters show the highest I_{ON} and peak transconductance G_{max} due to the reduced total resistance R_{tot}, while the smallest diameter devices yield the largest I_{ON}/I_{OFF} ratios and the smallest DIBL due to strong gate electrostatics. The source/drain asymmetry inherently exists in the vertical nanowire architectures. By swapping source and drain, electrical FOMs keep a similar trend in diameter scaling. I_{ON}, R_{tot} and G_{max} asymmetry can be attributed to top/bottom contact resistance difference resulting from the doping deactivation effect in small

nanowires. Low temperature dependence study shows that robust surface passivation and contacts in vertical nanowire transistors should be developed.

In this regard, lowering the contact resistance especially on the top of the small nanowires is found to be essential for performance enhancement. Here introducing a small bandgap GeSn material as the top layer is one practical way to reduce contact resistivity. The benefits of using GeSn are visible in strain and band structure simulation. With optimized nanowire patterning, excellent surface passivation, and NiGeSn metallization, GeSn/Ge achieves low *SS* of 67 mV/dec, small DIBL of 24 mV/V, and a high I_{ON}/I_{OFF} ratio of > 10^6. In addition, record-high $G_{m,ext}$ of ~870 μS/μm and the best quality factor *Q* of 9.1 are obtained for all reported GeSn-based pMOSFETs. Further performance comparison on nanowire diameter scaling and EOT scaling is conducted between GeSn/Ge heterostructure and Ge homojunction nanowire pMOSFETs, affirming the advantage of GeSn. All in all, the vertical nanowire architecture along with Ge(Sn) material embodies the significant potential for SiGeSn-based low power applications.

5. GeSn/Ge vertical GAA nanowire CMOS transistors and inverters

Contents

5.1. GeSn/Ge vertical GAA nanowire nMOSFETs

In chapter 4, Ge(Sn)-based vertical GAA nanowire pMOSFETs have been experimentally achieved and systematically studied. However, as an indispensable counterpart for CMOS applications, Ge(Sn)-based vertical nanowire nMOSFETs have not been realized yet. On one hand, the high electron mobility of Ge(Sn) is overshadowed due to a high D_{it} at the interface between a dielectric and Ge(Sn) channel, on the other hand, as is stated in session 3.5, the large Schottky barrier height Φ_B for electrons in the n-type Ge(Sn) metal contact results in large contact resistance, also hampering the satisfactory on-state performance. In this session, based on Ge n^+-n^--n^+ and Ge/$Ge_{0.95}Sn_{0.05}$/Ge n^+-n^--n^+ material stacks shown in Figs. 3.2 (c-d), Ge(Sn)-based vertical nanowire nMOSFETs are fabricated and characterized. The performance booster of the GeSn channel over Ge is also confirmed.

5.1.1. Material characterization and device fabrication

The fabrication of Ge/GeSn/Ge nanowire nMOSFETs starts with the epitaxy of Ge:P/GeSn/Ge:P stacks on 200 mm Si wafers by CVD growth, which is shown in the cross-sectional TEM image (Fig. 5.1 (a)). Each stack is ~100 nm thick. The good crystalline quality of Ge and GeSn layers and the defect-free interfaces are highlighted in Figs. 5.1 (b-c). The

pseudomorphic growth of the GeSn layer is also confirmed in the RSM (Fig. 5.2 (a)), the GeSn layer has the same in-plane lattice vector as Ge layers, while the peaks of the top and bottom Ge layers overlap, showing no degradation. Fig. 5.2(b) shows the TOF-SIMS depth profiles of P, Sn, and Ge elements along the epi-stacks. The *in-situ* P doping is clearly seen in the top and bottom Ge layers.

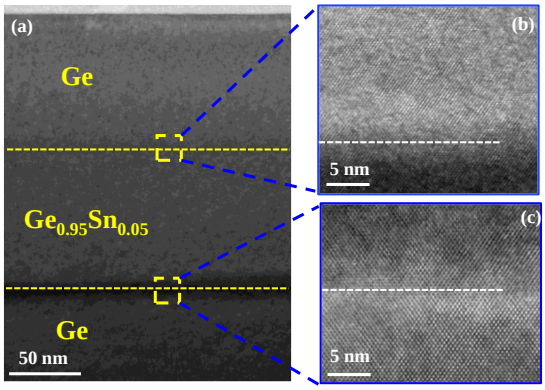

Fig. 5.1 (a) Cross-sectional TEM image of Ge/$Ge_{0.95}Sn_{0.05}$/Ge epi-stacks. HR-TEM images of Ge/$Ge_{0.95}Sn_{0.05}$ interface (b), and $Ge_{0.95}Sn_{0.05}$/Ge interface (c), highlighting the good crystallinity of GeSn and Ge layers, and defect-free interfaces.

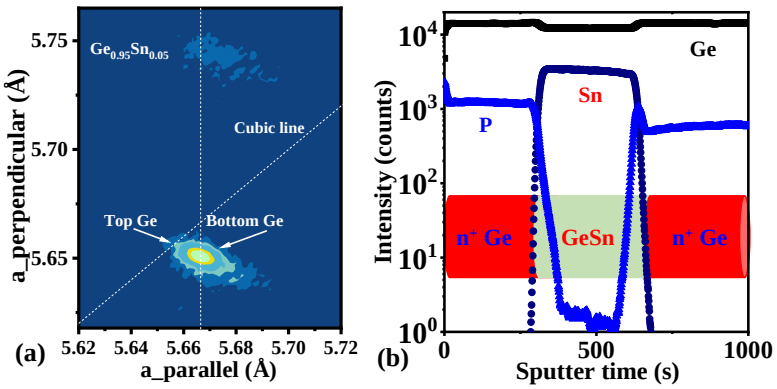

Fig. 5.2 (a) RSM of as-grown Ge/$Ge_{0.95}Sn_{0.05}$/Ge layers. The GeSn layer has the same in-plane lattice vector as the top and bottom Ge layers, showing the pseudomorphic growth. (b) TOF-SIMS analysis of P, Sn, and Ge elements along the epi-stacks. The *in-situ* P doping is clearly shown in the top and bottom Ge layers.

The activated Phosphorous doping distribution is measured with ECV (Fig. 5.3), showing doping concentrations of ~7×10^{19} and ~2.5×10^{19} cm^{-3} in the top and bottom layers of Ge/GeSn/Ge stacks, respectively. The higher P doping in the top layer is caused by the lower temperature and different growth chemistry considering the thermal budget constraints of GeSn. As a control sample of Ge homostructures, the top and bottom Ge layers have a doping

concentration of ~2.5×10^{19} cm^{-3}. The middle layer (channel part) is slightly n-type doped due to the memory effect during the growth. From this doping scheme, the devices indeed work in the accumulation-mode, which is notably desired for Ge(Sn)-based nMOSFETs.

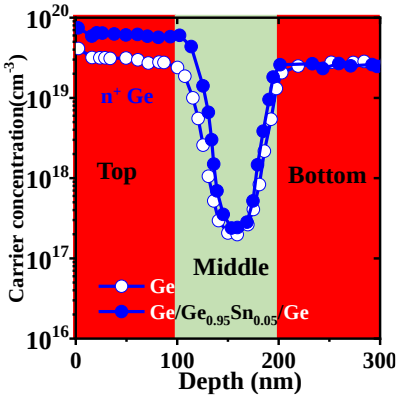

Fig. 5.3 ECV depth profiling of active dopants concentration along the epi-stacks. The top and bottom Ge layers in Ge:P/GeSn/Ge:P stacks show n-type doping concentrations of ~ 7×10^{19} and ~ 2.5×10^{19} cm^{-3}, respectively.

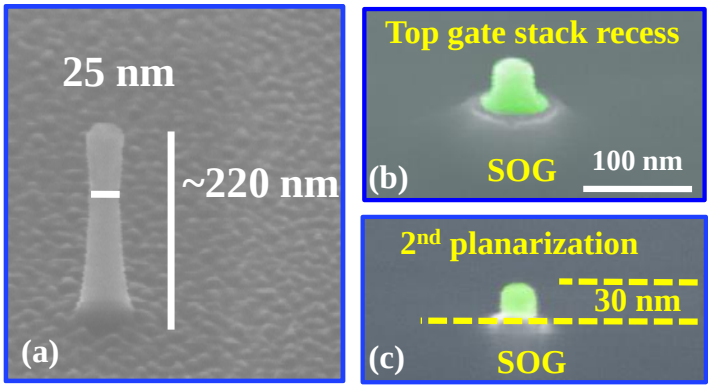

Fig. 5.4 (a) Tilted SEM image of a vertical Ge/GeSn/Ge nanowire with D = 25 nm, smooth sidewalls, and an aspect ratio of ~9. (b) The top gate stack recess process, the green region is the exposed top of a nanowire. (c) The second planarization, the top 30 nm is exposed for top contact metallization.

After the material growth, the fabrication of vertical Ge/GeSn/Ge nanowire nMOSFETs is conducted with the process similar to session 4.1. After Cl_2-based dry etching and digital etching, Fig. 5.4 (a) shows the tilted SEM image of a vertical nanowire with D = 25 nm and smooth sidewalls. It is noted that the rough planar surface is caused by the non-volatile $SnCl_x$ re-deposition during the 0 ℃ dry etching. Fig. 5.4 (b) shows the top gate stack recess process and a second planarization is conducted to isolate the gate stack and top contact (Fig. 5.4 (c)). Each process during device fabrication is carried out under a low thermal budget (< 400 ℃)

to avoid Sn segregation. As a comparison, Ge homojunction nanowire nMOSFETs are also fabricated with the same conditions. For these two devices, dielectric stacks of ~5 nm HfO_2/~1 nm Al_2O_3 are conducted with a post-oxidation process, resulting in an EOT of ~ 2.4 nm.

5.1.2. Electrical characterization

The electrical performance comparison between Ge homojunction and Ge/GeSn/Ge heterojunction nanowire nMOSFETs is conducted in Fig. 5.5. Fig. 5.5 (a) presents I_{DS}-V_{GS} transfer characteristics of a single Ge nanowire nMOSFET with D = 25 nm and L_G = 100 nm. It shows SS of 136 mV/dec and an I_{ON}/I_{OFF} ratio of ~1×10^4 at V_{DS} = 0.5V. These values are indeed comparable to the one reported for horizontal Ge nanowire nMOSFETs [61]. Improving the interface quality to suppress the high D_{it} and increasing n-type doping in the top/bottom stacks are required to further enhance the performance. While the Ge/$Ge_{0.95}Sn_{0.05}$/Ge nanowire nMOSFET with the same diameter exhibits better subthreshold properties with SS of 92 mV/dec and an I_{ON}/I_{OFF} ratio of ~6.6×10^4 (Fig. 5.5(b)). The performance enhancement with the GeSn channel is also reflected in the extrinsic transconductance $G_{m,ext}$ characteristics in Fig. 5.5(c). The peak G_{max} for GeSn-channel nMOSFET, ~480 µS/µm, is much higher than ~118 µS/µm for Ge nMOSFET. From the above analysis, the superiority of high-mobility GeSn as the channel over Ge is confirmed.

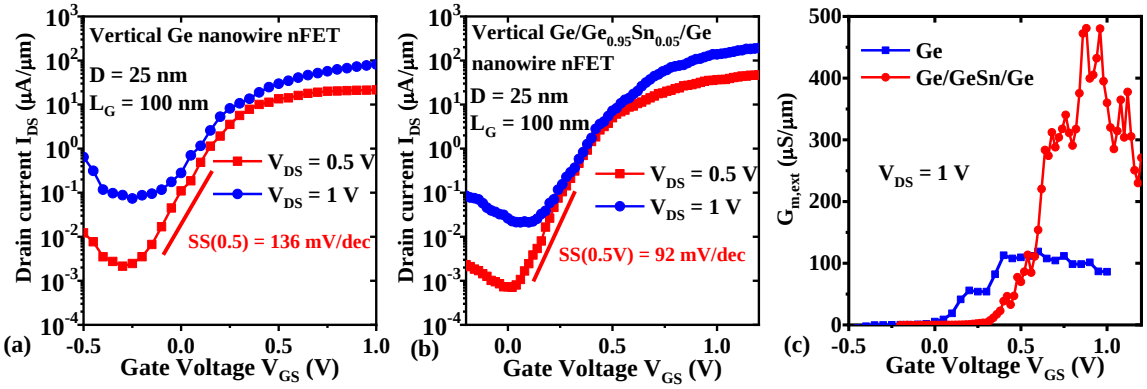

Fig. 5.5 (a) I_{DS}-V_{GS} transfer characteristics of a single Ge GAA nanowire nMOSFET with a diameter of 25 nm and a gate length of 100 nm: SS = 136 mV/dec, and an I_{ON}/I_{OFF} ratio = ~1×10^4 at V_{DS} = 0.5V. (b) I_{DS}-V_{GS} transfer characteristics of a vertical Ge/GeSn/Ge nanowire nFET with GeSn as channel and D = 25 nm: SS = 92 mV/dec, and an I_{ON}/I_{OFF} ratio = ~ 6.6×10^4 at V_{DS} = 0.5V. (c) Extrinsic $G_{m,ext}$ versus V_{GS} for Ge and GeSn-channel nMOSFETs at V_{DS} of 1V. Obviously, GeSn-based nMOSFETs exhibit higher $G_{m,ext}$ compared to Ge nMOSFETs.

The measurement above is in TCD configuration. Here source/drain asymmetry with both TCD and TCS configurations are also conducted for the GeSn-channel nMOSFETs with D = 25 nm. Fig. 5.6(a) compares the I_{DS}-V_{GS} curves at V_{DS} = 0.5V for both configurations. Apparently, the significant asymmetry in electrical behaviors, e.g. I_{ON}, *SS*, is observed. What is more, I_{DS}-V_{DS} curves with both configurations in Figs. 5.6 (b-c) also show the apparent difference in the turn-on behaviors and drain current saturation properties. Both devices show a typical super-linear onset and the phenomenon is much stronger for the device with TCD configuration, which is a strong indicator that the contact is Schottky. This would happen because the doping concentration of ~3×10^{19} cm^{-3} in the bottom Ge layer is not enough to form an Ohmic contact, as is already explained in Fig. 3.22. Moreover, the inferior *SS* in TCS supports that the top contact is also Schottky. Because from the source/drain asymmetry analysis in vertical Ge nanowire pMOSFETs in session 4.3.3, *SS* should behave similarly for both TCD and TCS, which is determined by the gate electrostatics. Here if the doping deactivation effect in small nanowires is included, a high doping concentration of ~7×10^{19} cm^{-3} in the top Ge layer could degrade, which results in a top Schottky contact, then it can be modulated by the applied gate/drain voltage, degrading the *SS* greatly for TCS configuration. Besides, the contact resistance difference results in the total resistance asymmetry for both devices. And the larger total resistance in TCS configuration results in better current saturation at low I_{DS} regime compared to TCD one (Fig. 5.6 (c)).

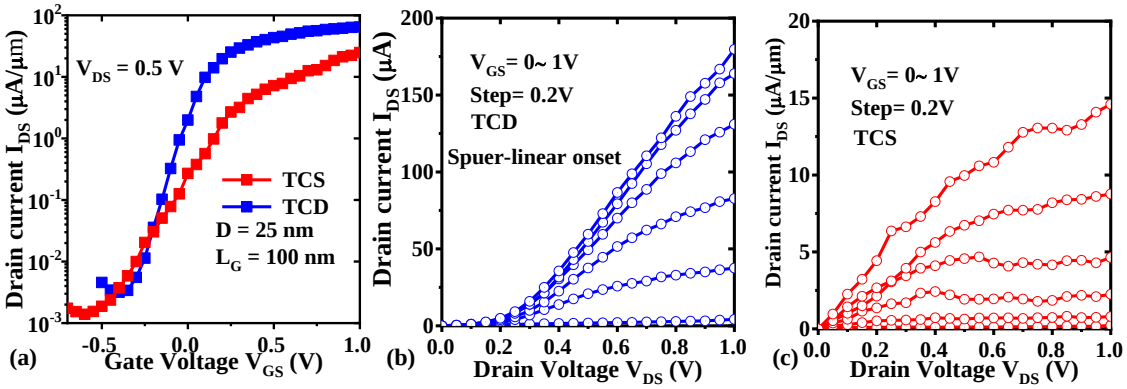

Fig. 5.6 (a) I_{DS}-V_{GS} transfer characteristics of a Ge/GeSn/Ge nanowire nMOSFET with TCS and TCD configurations. The significant asymmetry in electrical behaviors is observed. (b) I_{DS}-V_{DS} output curves for GeSn-channel nFET with TCD configuration (b) and TCS configuration (c). Both devices show typical super-linear onset properties.

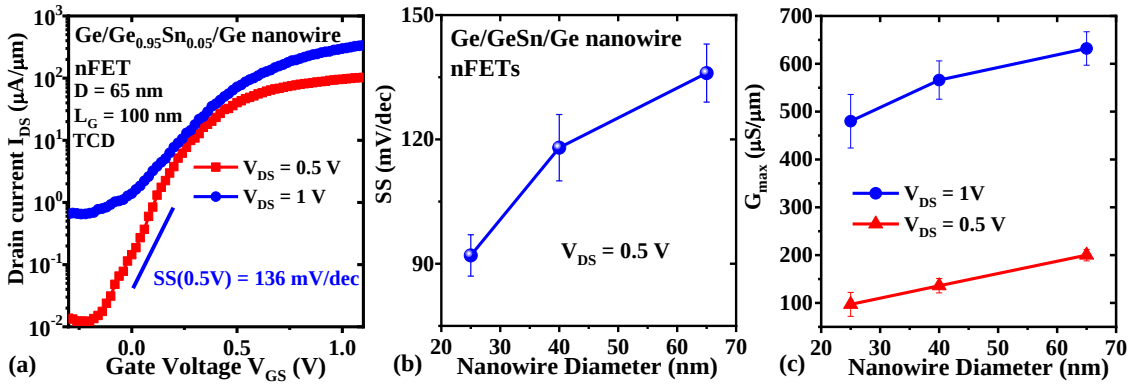

Fig. 5.7 (a) I_{DS}-V_{GS} transfer characteristics of a GeSn-channel nFET with a diameter of 65 nm: *SS* = 136 mV/dec, and G_{max} = ~ 632 μS/μm. (b) *SS* scaling metrics as a function of nanowire diameters for GeSn-channel nanowire nFETs at V_{DS} = 0.5V. *SS* decreases with diameters. (c) G_{max} with nanowire diameters for GeSn-channel nFETs measured at V_{DS} = 0.5V and 1V. Larger diameter devices show higher G_{max} due to smaller total resistances.

The largest 65 nm nanowire GeSn-channel nMOSFET is also fabricated and characterized in Fig. 5.7 (a) with TCD configuration. It exhibits SS of 136 mV/dec and peak G_{max} of ~ 632 μS/μm. SS scaling metrics as a function of nanowire diameters for GeSn-channel nanowire nMOSFETs are summarized in Fig. 5.7(b). As expected, SS shows a decreasing trend as the nanowire diameter shrinks due to improved gate electrostatics. Fig. 5.7(c) shows G_{max} versus nanowire diameters measured at V_{DS} = 0.5V and 1V. G_{max} becomes larger with increasing nanowire diameters because the total resistance R_{tot} becomes smaller due to the diameter-related top contact resistance. The G_{max} and R_{tot} scaling trends with nanowire diameters for nMOSFETs are consistent with those for Ge(Sn)-based pMOSFETs discussed in chapter 4.

5.2. GeSn-based vertical GAA nanowire CMOS inverters

So far, Ge(Sn)-based vertical GAA nanowire p-type and n-type MOSFETs have been experimentally achieved and electrically characterized. The goal in this subsequent chapter is to demonstrate the proof of concept for hybrid GeSn-based vertical nanowire CMOS inverters, which are basic building blocks of digital circuits. Although these CMOS transistors are not connected on the same chip-level but via the external cables and needles with two n- and p-type chips, they are taken as the first step to evaluate the feasibility of vertical nanowire MOSFETs in circuit applications. In future processing, the CMOS circuits should be monolithically integrated on the same chip. Combining GeSn-based n- and p-type transistors with symmetrical performance, the voltage transfer characteristics (VTC) of a hybrid inverter is analyzed. Further improvement for a good noise margin is also suggested.

5.2.1. Working principle of CMOS inverters

A CMOS inverter is a logical NOT gate that inverts the input voltage signal V_{IN} to the output $V_{OUT} = \overline{V_{IN}}$. For example, a high input level through the inverter can be converted into a low level and vice versa. Generally, the inverter can be performed only by using n-MOS or p-MOS logic MOSFET, but at the sacrifice of switching speed and power dissipation. Typically, in the digital circuits, complementary n- and p-type MOSFETs are used to form the CMOS inverter as is illustrated in Fig. 5.8 (a). The source terminal of the pMOSFET is connected to the supply voltage V_{DD}, while the source of the nMOSFET is grounded (GND). The input voltage V_{IN} is connected to the shared gate for n- and p-MOSFETs. And the output voltage V_{OUT} corresponds to the drain voltage for both devices. Based on the series connection with the shared input, complementary switching is enabled, which means either nMOSFET or pMOSFET is switched on by varying the applied V_{IN}. With a high input V_{IN}, the nMOSFET is activated and pulls the V_{OUT} down to the ground potential acting a pull-down transistor, on the other hand, by decreasing the V_{IN}, the pMOSFET will be on and pulls the V_{OUT} up to the V_{DD} level, which leads to the relation for pMOSFET $V_{GS}^{p} = V_{IN} - V_{DD}$. Therefore, the pMOSFET functions as a pull-up transistor.

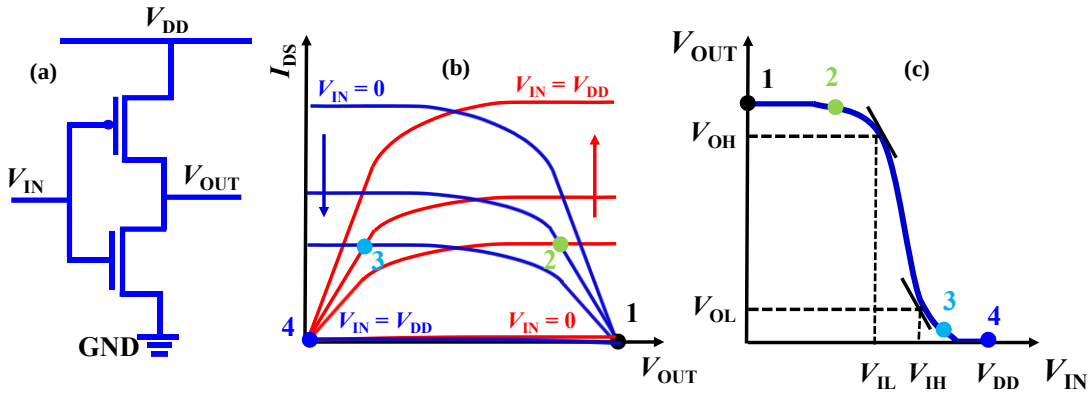

Fig. 5.8 (a) Schematic of a CMOS inverter. V_{DD} is the supply voltage and the input voltage V_{IN} is connected to the shared gate for n- and p-MOSFETs. (b) A load-line plot of the n- (red) and p-MOSFET (blue) of the CMOS inverter. The intersection of the load lines under the same V_{IN} determines the corresponding V_{OUT}. (c) Voltage transfer characteristics of the inverter with the corresponding intersection points.

The VTC graphically represents the relationship between V_{IN} and V_{OUT} of an inverter, which can be deduced from the superimposition of I_{DS}-V_{DS} output characteristics for n- and pMOSFETs. In order to achieve this load-line plot, several requirements have to be followed:

$$V_{IN} = V_{GS}^{n} = V_{GS}^{p} + V_{DD}$$

$$V_{OUT} = V_{DS}^{n} = V_{DS}^{p} + V_{DD} \tag{5.1}$$

$$I_{\mathrm{DS}}^{n} = -I_{DS}^{p}$$

Considering the above equations, such plots of load-line and VTC are depicted in Figs. 5.8 (b-c). The intersection of the load lines under the same V_{IN} determines the corresponding V_{OUT}. Several interception points are highlighted with different colors in Fig. 5.8(b). At black point 1, V_{IN} = 0V, the pMOSFET is on ($V_{GS}^{p} = V_{IN} - V_{DD}$) while the nMOSFET is off ($V_{GS}^{n} = 0$), therefore $V_{\mathrm{OUT}} = V_{\mathrm{DD}}$, the high voltage level is obtained, which can be reflected at point 1 in Fig. 5.8 (c). The green point 2 reaches the state before V_{OUT} flips. The nMOSFET is switched on but the drain current of the pMOSFET is still in the linear region. The inverter changes its state at point 3. Point 4 means the standby state with $V_{\mathrm{IN}} = V_{\mathrm{DD}}$, the pMOSFET is off and the nMOSFET is on. One interesting point in the VTC is called the switching threshold V_{M} of the inverter at $V_{\mathrm{IN}} = V_{\mathrm{OUT}} = V_{\mathrm{DD}}/2$. Both devices at this point operate in the saturation region where a minor change of V_{IN} can lead to a large V_{DD} variation. This transition of an inverter can be gradual and extends to the points where the slope of the VTC (voltage gain) reaches$\frac{dV_{IN}}{dV_{OUT}} = -1$. Meanwhile, this also sets two boundary points (V_{IL}, V_{OH}) and (V_{IH}, V_{OL}) as shown in Fig. 5.8 (c). An input voltage V_{IN} below V_{IL} is considered as a low-level input while V_{IN} above V_{IH} is a high-level input. The voltage range where a maximum variation cannot flip the states is called noise margin (NM). $\mathrm{NM_{H/L}}$ for the high or low input state can be quantified as:

$$NM_H = V_{OH} - V_{IH} \tag{5.2}$$

$$NM_L = V_{IL} - V_{OL} \tag{5.3}$$

For $\mathrm{NM_H}$, it can be interpreted that the high output voltage V_{OH} of the first inverter should be large enough so that V_{IN} of the second inverter in series is above V_{IH}. The same approach also goes to $\mathrm{NM_L}$.

For the perfect inverter, the noise margin can extend the whole voltage swing, providing a maximum $V_{\mathrm{DD}}/2$ for high and low input state. This requires an abrupt transition between the two logical states, which means a large gain. Excellent current saturation and the steep current increase in the linear regime in I_{DS}-V_{DS} output characteristics can approach this purpose. What

is more, high on-state currents of both n- and p-transistors guarantee fast switching of the inverter.

5.2.2. GeSn-based hybrid nanowire CMOS inverter

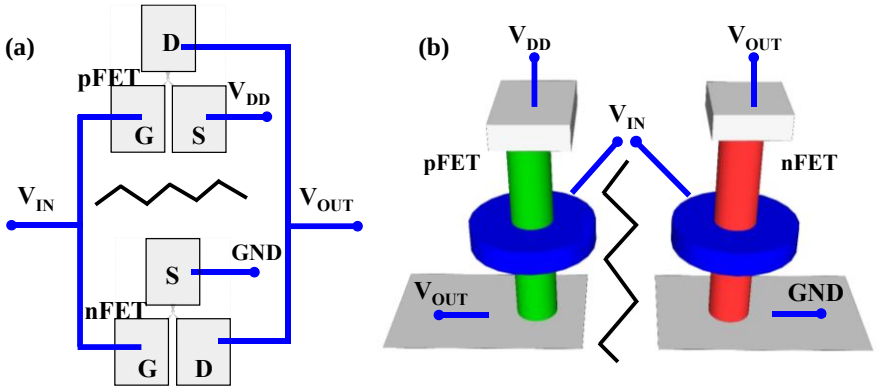

Fig. 5.9 (a) Top-view layout of connected p- and n-MOSFETs for a hybrid nanowire CMOS inverter. (b) 3D schematic of the connected inverter. V_{DD} is connected to the top source contact of pMOSFET and GND is grounded to the bottom source contact of nMOSFET.

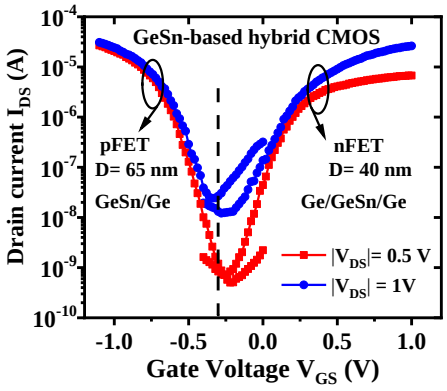

Fig. 5.10 I_{DS}-V_{GS} transfer characteristics of the GeSn-based pMOSFET and nMOSFET to form a hybrid nanowire CMOS inverter. The transfer curves of both devices are symmetric at around -0.3V in terms of I_{ON}, *SS*, and DIBL.

GeSn-based vertical GAA nanowire p-type and n-type MOSFETs with symmetrical performance are selected to form hybrid nanowire CMOS inverters via the external connection. Although large impedances and parasitic capacitances are included, in this case, only DC operation on the inverter is conducted. As is shown in Fig. 5.9 (a), it is a top-view layout of connected p- and n-MOSFETs. For the GeSn/Ge pMOSFET, it adopts TCS configuration while for the Ge/GeSn/Ge nMOSFET, it utilizes TCD configuration for a better performance match. Fig. 5.9 (b) is the 3D schematic of the connected inverter. V_{DD} is

connected to the top source contact of pMOSFET and GND is grounded to the bottom source contact of nMOSFET.

The normalized I_{DS}-V_{GS} transfer characteristics of GeSn-based vertical nanowire p- and n-type MOSFETs forming a hybrid inverter are plotted in Fig. 5.10, in which a pMOSFET with D = 65 nm and a nMOSFET with D = 40 nm are chosen. Both devices show symmetric transfer curves at around -0.3V in terms of I_{ON}, *SS*, and DIBL, necessary conditions to enable good switching for the inverter. This means the switching threshold of the inverter will have a shift of -0.3V in the VTC. The gate metals with appropriate work-functions for n- and p-FETs can be adjusted to make the performance symmetry at 0V. The I_{DS}-V_{DS} output characteristics for each device are measured at $|V_{GS}|$ sweeping from 0V to 1V in Fig. 5.11. The pMOSFET exhibits good pinch-off property and achieves ~21 μA at V_{GS} =-1V, while a typical super-linear onset property for small V_{DS} in nMOSFET is observed due to the low n-type doping concentration in the top/bottom Ge layers.

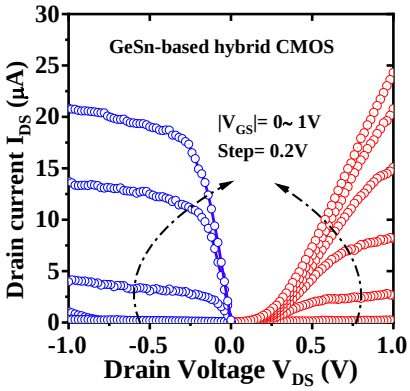

Fig. 5.11 The I_{DS}-V_{DS} output characteristics for each device are measured at $|V_{GS}|$ sweeping from 0V to 1V

The VTC for the hybrid nanowire CMOS inverter is recorded for V_{DD} from 1V to 0.2V shown in Fig. 5.12 (a). Because of the negative shift of I_{DS}-V_{GS} curves, V_{IN} has to be adjusted to allow the complete switching of the inverter. A sharp transition at around -0.3V + V_{DD}/2 is observed for each curve, even at a very small V_{DD} of 0.2V. Obviously, the VTC exhibits two distinct logical states for low and high V_{IN}. At a low V_{IN} regime, V_{OUT} reaches the maximum logical level (V_{DD}). However, at high V_{IN}, the VTC shows an apparent degradation. This is caused by the strong GIDL effect for pull-up pMOSFETs as shown in Fig. 5.10. Because for GeSn/Ge pMOSFET with TCS configuration, the gate stack directly sits on the bottom plane, which increases the overlapping area between the gate and bottom drain region, thus it leads to severe GIDL effect. For instance, at a V_{IN} = 0.7V and V_{DD} = 1V, the nMOSFET turns on

and tries to pull V_{OUT} down to GND, but the increased current caused by GIDL prevents the V_{DD} from reaching GND. However, the GIDL effect for the nMOSFET with TCD configuration is less pronounced, resulting in a good NM_L. What is more, under the same V_{IN} and larger V_{DD}, V_{GS}^{p} gets more positive, giving rise to a stronger GIDL effect and consequently further increasing V_{OUT}. Further improvement can be implemented by the gate self-alignment with respect to the channel by the deposition of a bottom insulator spacer in GeSn/Ge pMOSFET, which is highlighted in the inset in Fig. 5.12(b). This bottom spacer can significantly reduce the capacitance coupling between the gate and bottom drain. Fig. 5.12(b) shows the corresponding voltage gain for various V_{DD} extracted from Fig. 5.12(a). A maximum voltage gain ~18 is achieved at V_{DD} = 0.8V. Decreasing V_{DD} leads to a smaller gain. At V_{DD} of 0.2V, the gain can still reach ~6, which demonstrates the potential for low power applications.

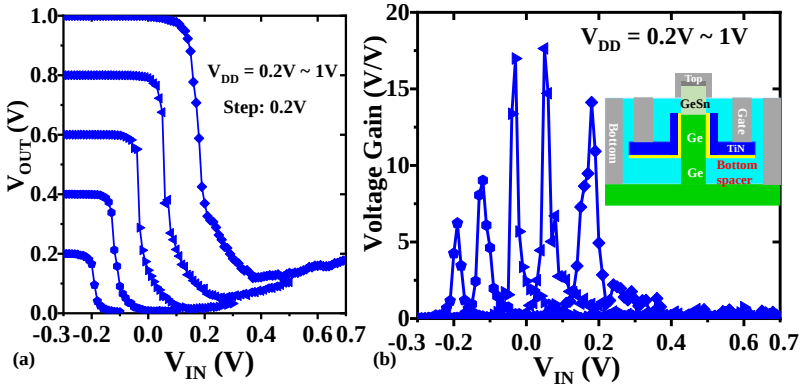

Fig. 5.12 (a) VTC of a hybrid inverter by varying the supply voltage V_{DD} from 0.2 V to 1 V. At high V_{IN} regime, V_{OUT} rises up, especially for high V_{DD} due to the obvious GIDL effect for pFETs. (b) Voltage gain versus V_{IN} of the inverter with a maximum gain of 18V/V at V_{DD} = 0.8V. Further voltage gain improvement can be implemented by the gate self-alignment with respect to the channel by the deposition of a bottom spacer (inset).

Benchmark

Fig. 5.13 benchmarks the maximum voltage gain for vertical nanowire inverters based on group III-V and IV materials. These nanowires are patterned either by top-down or bottom-up methods. So far, only a few reports are found on vertical nanowire inverters considering the challenging processing of integrating n- and p-MOSFETs on the same chip [100, 234-236]. With a novel bottom-up growth for InAs and InAs/GaSb vertical nanowires, J. Svensson *et al*. demonstrated monolithic integration of both n-type and p-type MOSFETs although a low gain of ~2 V/V was obtained due to the averaged-behaved performance [235]. Y. Guerfi

et al. utilized the ion implantation method to pattern n-type and p-type Si nanowires on the same chip and achieved a gain of ~11 [100]. Nevertheless, this work demonstrates the first proof of concept for a hybrid GeSn-based nanowire inverter via external connection, and a high voltage gain of ~18 is obtained. Advanced process, e.g. selective epitaxy to pattern both n-type and p-type vertical nanowires are required to monolithically integrate on the same chip for very-large-scale integration (VLSI) applications.

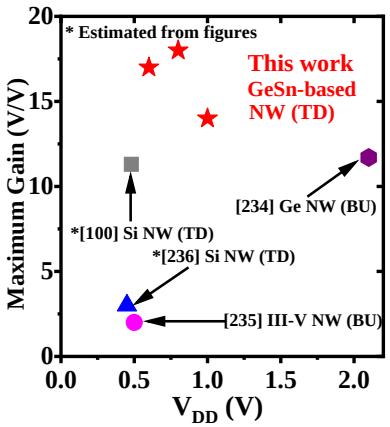

Fig. 5.13 Benchmark of voltage gain for vertical nanowire inverters based on group III-V and IV materials. The nanowires are patterned either by top-down (TD) or bottom-up (BU) methods. This work demonstrates higher maximum gain at relatively lower V_{DD} for GeSn-based nanowire CMOS inverters.

5.3. Conclusion

In this chapter, with the well-developed process flow, vertical Ge/$Ge_{0.95}Sn_{0.05}$/Ge GAA nanowire nMOSFETs with diameters down to 25 nm are obtained with decent electrical results, which outperform Ge control nMOSFETs. GeSn-channel nanowire nMOSFETs with D = 65 nm achieve a high G_{max} of ~ 632 µS/µm. The *SS* and $G_{m,ext}$ scaling trends demonstrate the dependence of gate electrostatic control and total resistance on nanowire diameters. The performance analysis suggests the plausible route for further improvement, which is increasing the n-type doping concentration in Ge layers, for instance by laser annealing or flash lamp annealing.

Combining Ge/$Ge_{0.95}Sn_{0.05}$/Ge nanowire nMOSFETs and $Ge_{0.92}Sn_{0.08}$/Ge nanowire pMOSFETs, the first proof of concept for a GeSn-based hybrid CMOS inverter is realized with a high voltage gain of ~18 at V_{DD}=0.8V. Advanced processing of the gate self-alignment towards source/drain is preferred to suppress the GIDL effect of both n- and p-MOSFETs and

also improve the noise margin for the inverter. The optimization of Ge(Sn)-based CMOS inverter will be focused on the monolithic integration of CMOS transistors. In short, this work demonstrates the great potential of GeSn-based nanowire MOSFETs for CMOS applications beyond 5 nm nodes.

6. Summary and outlook

Within the scope of this thesis, GeSn/Ge vertical GAA nanowire MOSFETs and CMOS inverters for ultra-low power logic applications are investigated. The vertical nanowire architecture presented here could provide the ultimate scalability with strong electrostatics and excellent immunity against short-channel effects. This design also provides the possibilities of band structure engineering, as well as convenient material epitaxy with *in-situ* doping. With the superior properties of Ge(Sn), the combinations would enable tremendous device and circuit explorations to extend the CMOS roadmap.

Complete process flow and key modules for vertical GAA nanowire transistors are introduced. Optimized dry etching and digital etching are developed to pattern nanowires with good verticality and smooth sidewalls. With these schemes, a small nanowire with a 20 nm diameter and an aspect ratio of ~10.5 is obtained. HSQ planarization is utilized to form the spacer insulation. Moreover, p-type and n-type Ohmic contacts for Ge(Sn) are pointed out for high-performance transistors. These process modules make it possible to demonstrate GeSn/Ge vertical GAA nanowire MOSFETs and evaluate the functionality and scaling technology of such devices.

Vertical Ge GAA nanowire pMOSFETs by a top-down approach are demonstrated for the first time in this thesis. Thanks to many well-functioning devices, the classical nanowire diameter-scaling properties could be evinced exhibiting a strong relationship with gate electrostatic integrity. The devices with 65 nm diameters show the highest I_{ON} and peak transconductance G_{max} due to the reduced total resistance R_{tot}, while the smallest diameter devices yield the largest I_{ON}/I_{OFF} ratios and the smallest DIBL due to improved gate electrostatics. One noteworthy point is the smallest nanowire devices exhibit slightly large parameter variability in key FOMs. It is primarily attributed to the potential variation of nanowire diameter uniformity, sidewall roughness, and surface passivation. The solutions are to develop robust nanowire patterning methods or adopt some variability-tolerated circuit designs before the implementation of GAA nanowire devices into volume production. Besides, how to lower the contact resistance in ultra-scaled nanowire transistors is a major obstacle for decent on-state performance. For vertical nanowire architecture, there is an inherent asymmetry between source and drain due to the difference in contacts, which has to be taken into account in circuit design. By swapping source and drain, electrical FOMs keep a similar trend in diameter scaling. I_{ON}, $R_{tot,}$ and G_{max} asymmetry originate from top/bottom contact resistance difference due to the doping deactivation effect in small nanowires. The

study of low-temperature measurement highlights the significance of surface passivation and contacts in vertical Ge nanowire transistors, especially for cryogenic applications.

Based on the analysis from Ge homojunction nanowire pMOSFETs, introducing a small bandgap GeSn material as the top layer is adopted to reduce contact resistivity. The benefits of GeSn/Ge heterojunction in the quasi-1D nanowires are demonstrated through strain and band structure simulation. The in-plane strain becomes largest at the GeSn/Ge interface and decays exponentially along the nanowire axis. Furthermore, smaller vertical GeSn/Ge nanowires become less strained, providing an effective option to relieve lattice mismatch coherently for hetero-epitaxy. A valence band offset ΔE_v existing at the $Ge_{0.92}Sn_{0.08}$/Ge heterojunction is beneficial to suppress the DIBL effect in pMOSFETs. Besides, the dependence of key FOMs on nanowire diameter scaling for GeSn/Ge pMOSFETs follows a similar trend as Ge pMOSFETs. With a scaled EOT, excellent surface passivation, and NiGeSn metallization, GeSn/Ge nanowire pMOSFETs achieve low *SS* of 67 mV/dec, small DIBL of 24 mV/V, and a high I_{ON}/I_{OFF} ratio of > 10^6. Record high $G_{m,ext}$ of ~870 µS/µm, and the best quality factor *Q* of ~ 9.1 are obtained among all reported GeSn-based pMOSFETs.

As a counterpart for CMOS applications, vertical Ge/$Ge_{0.95}Sn_{0.05}$/Ge GAA nanowire nMOSFETs with diameters down to 25 nm are realized with decent electrical results. GeSn-channel nanowire nMOSFETs achieve *SS* of 92 mV/dec and peak $G_{m,ext}$ of ~ 632 µS/µm, which outperform Ge control nMOSFETs and confirm the superiority of high-mobility GeSn as the channel. The performance-symmetrical Ge/$Ge_{0.95}Sn_{0.05}$/Ge nanowire nMOSFETs and $Ge_{0.92}Sn_{0.08}$/Ge nanowire pMOSFETs are selected to form the first proof of concept for a GeSn-based hybrid CMOS inverter via the external connection, which achieves a high voltage gain of ~18 at V_{DD}=0.8V. A sharp transition at around -0.3V + V_{DD}/2 is observed even at a very small V_{DD} of 0.2V. To improve the noise margin for the inverter, the gate self-alignment towards source/drain is preferred to suppress the GIDL effect of n- and p-MOSFETs. In short, this work demonstrates the significant potential of GeSn-based nanowire MOSFETs for CMOS applications beyond 5 nm nodes.

To fully exploit the great advantage of vertical nanowire architecture along with Ge(Sn) material, robust transistor fabrication schemes are required before it is competitive with Si CMOS devices. Specifically for p-type and n-type Ge(Sn), high-quality material growth, sufficient surface passivation, and excellent Ohmic contacts are priorities to be tackled. Besides, sub-10 nm nanowire transistors are needed beyond 5 nm nodes. Optimization on ultra-scaled nanowire patterning, top contact metallization, and gate self-alignment is worth the effort for manufacturing. Moreover, metrology methods for ultra-scaled nanowire characterization and capacitance property on vertical nanowire MOScap are also required.

The vertical nanowire architecture as well as Ge(Sn) material embodies the significant potential for SiGeSn-based low power applications. Based on this work, to complement vertical nanowire transistors with beyond-CMOS counterparts, e.g. memory, photonics is quite promising for monolithic 3D integration. All in all, there is plenty of room to be explored in the era of 3D IC.

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Conference contributions

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